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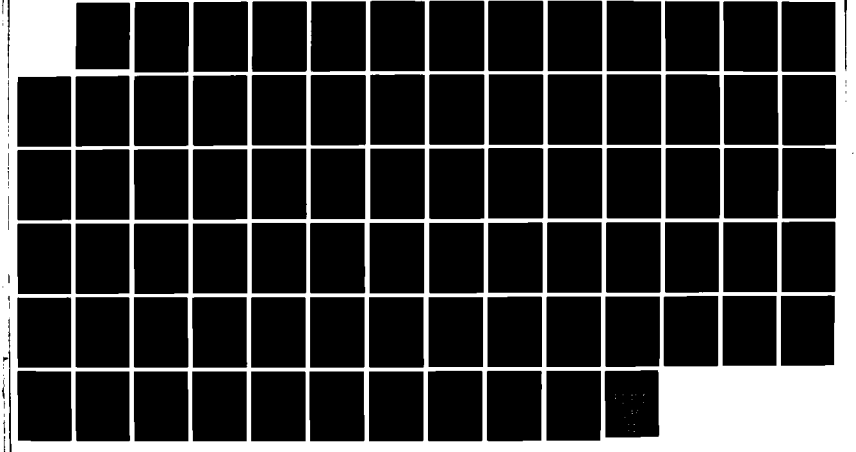

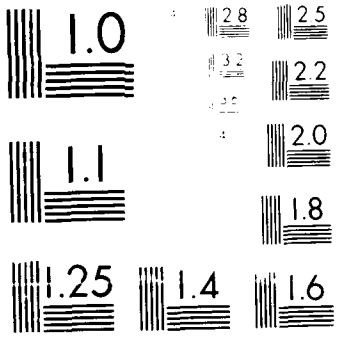
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THE ANALYSIS OF CURRENT-MIRROR MOSFETs FOR USE IN RADIATION ENVIRONMENTS

by

Marino Juan Martinez

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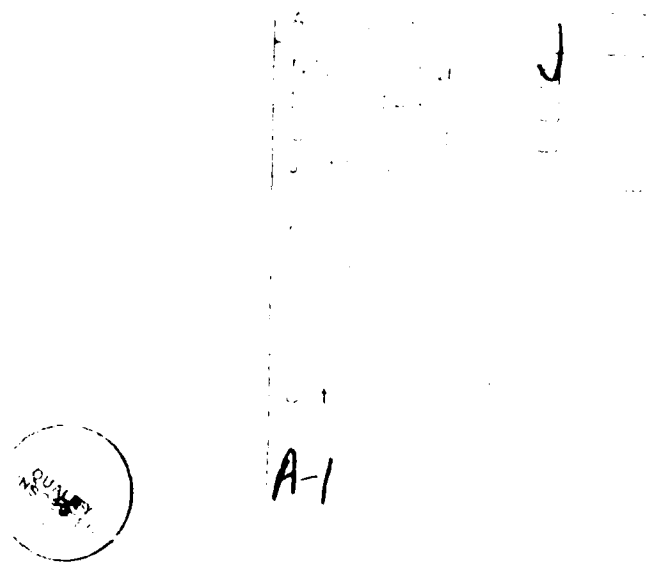

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ABSTRACT

Experiments were conducted on current-mirror MOSFETs to examine their suitability for use in radiation environments. These devices, which allow low loss load current sensing (defined by a current-ratio a'), are an important element of many power integrated circuits (PICs). Total-dose testing demonstrated that the current ratio was virtually unaffected for many operating conditions. In all cases, changes were largest when sense resistance was largest and minimal when sense voltage was approximately equal to the load source's voltage. In addition, testing verified the feasibility of using sense-cell MOSFETs for applications which require radiation exposure. A constant-current op-amp circuit showed minimal current shifts, using proper circuit design, following total-dose exposure. Dose-rate testing showed the feasibility of using sense voltage to trigger $\dot{\gamma}$ protection through drain-source voltage clamping, providing a relatively inexpensive alternative to voltage derating.

CHAPTER 1: INTRODUCTION

SECTION 1.1: MOTIVATION

The effects of radiation environments on power MOSFET devices is a well established area of research [1,2,3,4]. This is especially true for applications in space-based systems such as satellites. The objective of such research is usually to examine how device structure, processing, and use may be changed to extend the useful life of these devices in radiation environments. However, some of the new power integrated circuits (PICs) show significant potential for application in such environments since they integrate both power and control elements in a single device, allowing identical or improved performance using less weight, volume, and power. Therefore, it is desirable to examine the effects of radiation on the operation of these new devices. Such an examination requires looking at changes at both the device level, as is usually the case, and the circuit level. Because PICs include control elements, there exists a possibility that in some cases these control elements may be utilized to maintain useful circuit operation under the changing conditions caused by a radiation environment, such as compensation for total-dose effects or protection against dose-rate upset. This becomes, in essence, a circuit level approach to radiation hardening. Naturally, the key to such an approach is that the performance of the control elements remains stable under any changes induced by radiation. Additionally, it is important to determine whether the normal control functions of PICs are impaired by exposure for those cases where these functions are not used for direct radiation hardening. This would help determine if the advantages of PICs can be used in such environments.

For this study, the subject was a device important to many PICs which is known by a number of different names: SenseFET*, HexSense**, Current-Mirror FET (CMFET), or sense-cell MOSFET. The particular device studied was the Motorola MTP10N25M SenseFET* power transistor, but the results should apply equally well to all such devices. To examine this particular device, one must have a basic understanding of DMOS devices, basic radiation effects in MOS devices, the

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* SenseFET is a registered trademark of Motorola, Inc.

** HexSense is a registered trademark of International Rectifier, Inc.

operation and use of the device, and the method of verifying predictions, that is, an experimental plan or procedure.

SECTION 1.2: DMOS DEVICES

Double-diffused Metal-Oxide-Semiconductor (DMOS) Field Effect Transistor devices are the most common form of MOS power devices since their attributes are especially well suited for power applications, as will become apparent. A representative structure of two cells of a vertical DMOS device is shown in Figure 1.

The name given DMOS devices is derived from the use of two diffusion steps to create the n^+ and p regions shown in the figure. The principal difficulty of the DMOS process is in obtaining a consistent threshold voltage from device to device. This is a consequence of the fact that instead of a constant doping level under the gate, there exists a doping profile which is determined by the two diffusion steps. This results in a profile such as that shown in Figure 2. This figure shows that the threshold voltage will depend on the peak doping value, $N_{A,max}$. This value will be controlled by the details of the diffusion steps, but the greatest variations come from differences in the predeposition step of the p-diffusion. If ion implantation is used in this predeposition step, reasonably good control of the threshold voltage is possible [6].

Nonetheless, DMOS devices are not without their advantages. One of these advantages is that the channel length is determined by the difference in lateral diffusion distances rather than the minimum dimension available from photolithography. Since there has traditionally been better control of diffusion distances than the dimensions of photolithographic openings, this structure allows shorter channel lengths than in the type of structure used for most MOS devices. In addition to this, the device density that is possible using a vertical DMOS structure can result in very large equivalent aspect ratios (channel width/channel length) which allows large currents to be controlled by a device which is small in surface area. It is this attribute which makes the DMOS structure a useful one for power devices.

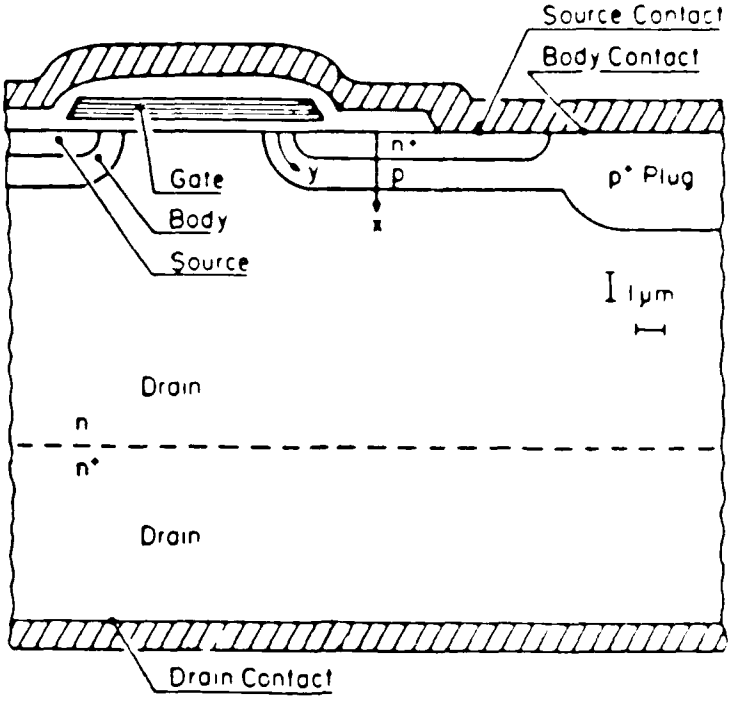

Figure 1: DMOS structure showing parasitic bipolar (After Hohl and Galloway [5])

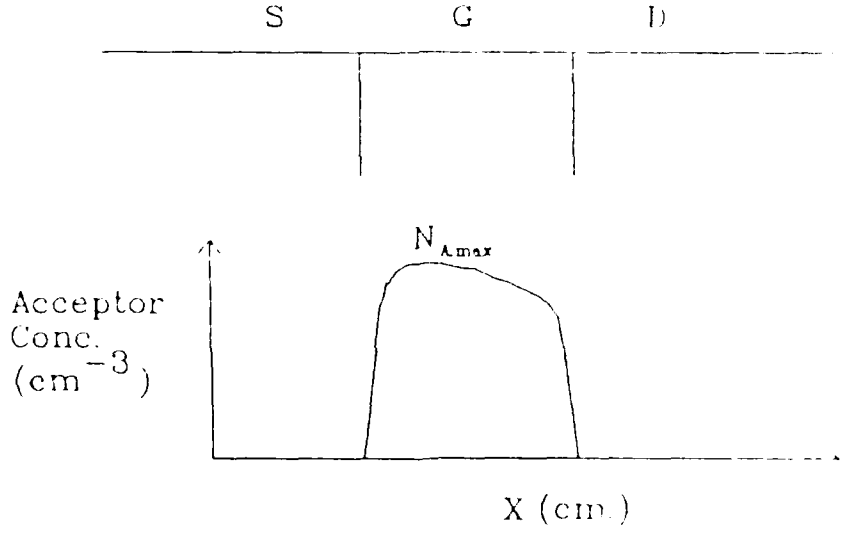

Figure 2 [After Pocha, et al. [1]]

Another important feature of DMOS power devices is that, on a given die, characteristics are very closely matched from cell to cell. This means that for the same gate-to-source and drain-to-source voltages, the current flowing in each cell will be very nearly the same. As will be shown, this attribute is essential to the creation of devices like the CMFET.

SECTION 1.3: THE CMFET

In a conventional DMOS power transistor, all the source contacts are tied in parallel to a single source pin. In such a device, the close matching of the cells means that the total current is approximately the current of a single cell multiplied by the number of cells. However, using a different metalization pattern, it is possible to split off the source connections of a subset of cells. The ratio of the currents in the different source branches will then be equal to the ratio of the number of cells in each branch, provided that the sources return to the same potential. This is shown in Figure 3, where the ratio of cells is n. This structure is exactly that of the CMFET. In the CMFET, a few of the cells are tied together to a separate source pin which is labelled by **M** for mirror. If both the main (load) and mirror (sense) source connections are returned to ground, then the current in the sense branch will be n times smaller than that in the load branch because of the previously mentioned matching between the DMOS cells [7,8,9,10].

Normally, however, it is preferable to use voltages rather than currents as indicators of circuit conditions. To obtain a voltage, a resistor can be inserted between the sensing source connection and ground, resulting in the circuit of Figure 4. Naturally, the voltage created by this resistor will alter the ratio of currents between the two branches since it alters the drain-source and gate-source voltages in the sense branch. Nonetheless, this is not a great problem because the ratio changes in a predictable fashion. This new ratio can be calculated easily using the simple square-law equations for the linear region of operation [9]. From this model, the drain current is given by

$$I_D = 2K[(V_{G1} - V_T)V_{DS1} - \frac{1}{2}V_{DS1}^2], \qquad (1$$

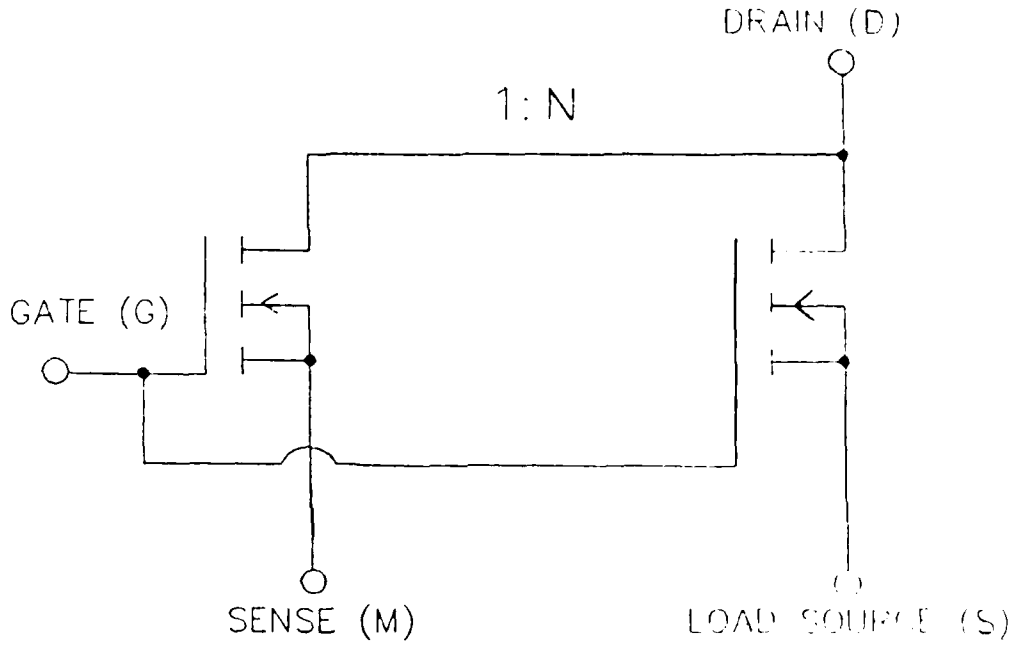

Figure 3: Schematic CMFET (After Schultz [8])

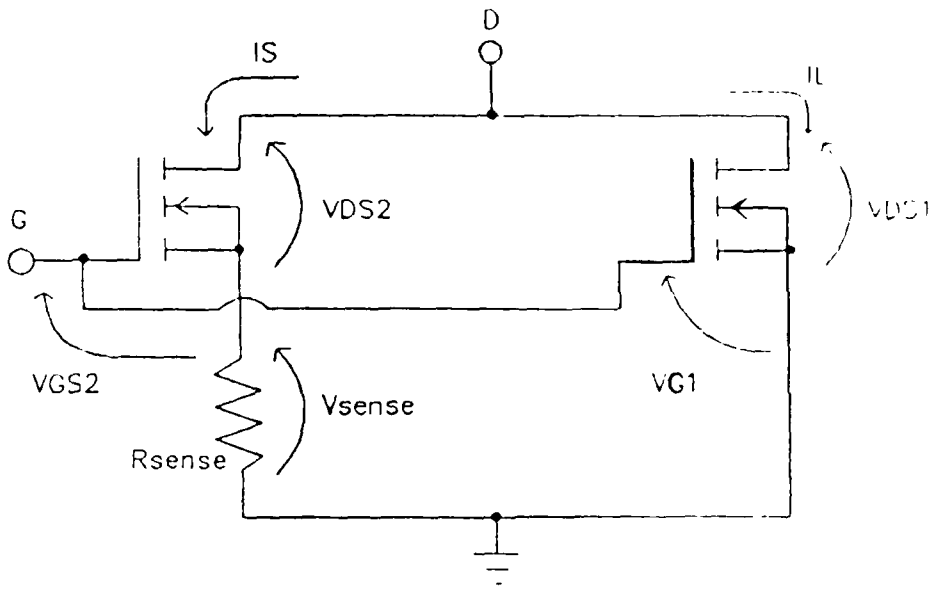

Figure 4: Typical CMFET Connection (After Fay [9])

where K is the channel conductivity of the device of the device and the voltages are defined in Figure 4. For the sense current, the important voltages are found from Figure 4 to be

$$V_{DS2} = V_{DS1} - V_{Sense} \qquad \text{and} \tag{2}$$

$$V_{G2} = V_{G1} - V_{Sense}. \tag{3}$$

Therefore, the sense and load currents are given by

$$I_{Sense} = 2K_S[(V_{G1} - V_{TS} - V_{Sense})(V_{DS1} - V_{Sense}) - \frac{1}{2}(V_{DS1} - V_{Sense})^2] \tag{4}$$

and

$$I_L = 2K_L[(V_{G1} - V_{TL})V_{DS1} - \frac{1}{2}{V_{DS1}}^2]. \tag{5}$$

The relation between K_S and K_L is easily found to be

$$K_L/K_S = n, \tag{6}$$

where n is the cell ratio. The new cell ratio, n', is found to be

$$\begin{aligned} n' = I_L/I_S &= \frac{2K_L[(V_{G1} - V_{TL})V_{DS1} - \frac{1}{2}{V_{DS1}}^2]}{2K_S[(V_{G1} - V_{TS} - V_{Sense})(V_{DS1} - V_{Sense}) - \frac{1}{2}(V_{DS1} - V_{Sense})^2]} \\ &= \frac{n}{1 - \frac{V_{Sense}(V_{G1} - V_T - \frac{1}{2}V_{Sense})}{V_{DS1}(V_{G1} - V_T - \frac{1}{2}V_{DS1})}} \end{aligned} \tag{7}$$

if the threshold voltages are assumed to be equal in both sections of the devices, as is approximately true. All the terms in this new expression, except the threshold voltages, are determined by the user of the device. A choice of V_{Sense} corresponding to a particular load current fixes the sense resistor value according to the relation

$$R_{Sense} = \frac{V_{Sense}n'}{I_{Load}}. \tag{8}$$

As might be expected, the choice of sense resistor and voltage values has a definite impact on the accuracy of the sense current. In other words, the ratio n' will not be constant for all conditions once the sense resistor value becomes fixed. Furthermore, the amount of variation is directly dependent on the sense resistor

value. The two most important aspects of accuracy are those dealing with linearity and temperature coefficient of n', although it will be shown that the sense resistor value also has an impact on performance in radiation environments.

The quality of linearity in the sense current means that it should vary linearly with the load current. For example, if V_{Sense} =1 V for I_L =10 A, then V_{Sense} =0.1 V for I_L =1 A. Unfortunately, the relation can never be exactly linear; that is, n' is never exactly constant for different conditions once R_{Sense} is fixed. The reason true linearity can never be achieved is that such a condition would require a device which varies linearly with gate voltage, and it is well known that MOSFETs approximately obey a square-law with respect to gate voltages, not a linear relation. It becomes clear that to achieve the greatest possible linearity, the gate-source and drain-source voltages must be as closely matched as possible in the sense and load sections of the CMFET. This requires the use of as small a value as possible for the sense resistor. This requirement is easily shown by observing that, in the limit of $R_{Sense} = 0$, true linearity is achieved if the cells are truly matched. It can be shown that, for small values (approximately 10% of the sense section on-resistance) of R_{Sense}, true linearity is approximated very closely [8,11].

Changes in n' due to changes in temperature are best explained using the equivalent on-resistance model of the CMFET circuit shown in Figure 5. In this circuit, $r_{dm(on)}$ = sense cell on-resistance = $nr_{ds(on)}$, where $r_{ds(on)}$ is the load section on-resistance. It is well-known that the on-resistance of a MOSFET changes with temperature, and for this device, both on-resistances will change by the same factor if the cells are well-matched. It is readily apparent from Figure 5 that if R_{Sense} does not change by the same factor as the on-resistances, the ratio of currents in the two branches must change. It is easily shown that this effect is minimized for small values of R_{Sense} [8,9,11]. Figure 6 shows the relationship between the value of R_{Sense} and accuracy of the current ratio n' under a thermal excursion.

Of course, there is a limit to how small R_{Sense} can be allowed to become. This limit is due to two primary considerations, circuit noise and useful sense voltage levels. In consideration of noise, the user must recognize that very small values

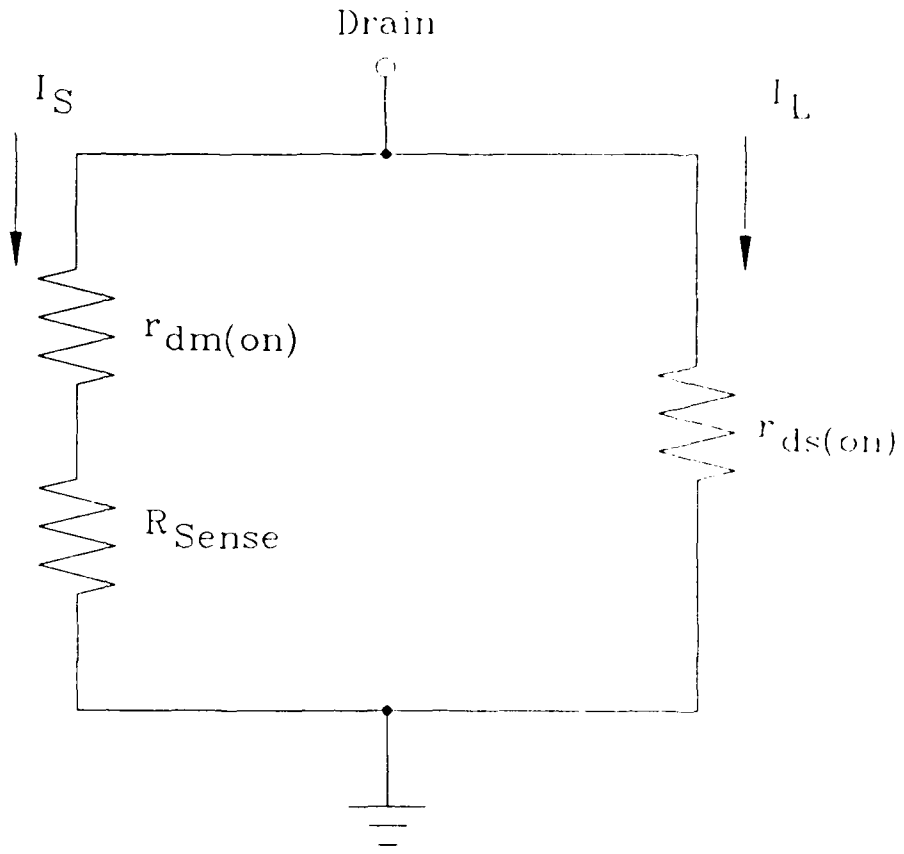

Figure 5: On-Resistance Model (After Fay [9])

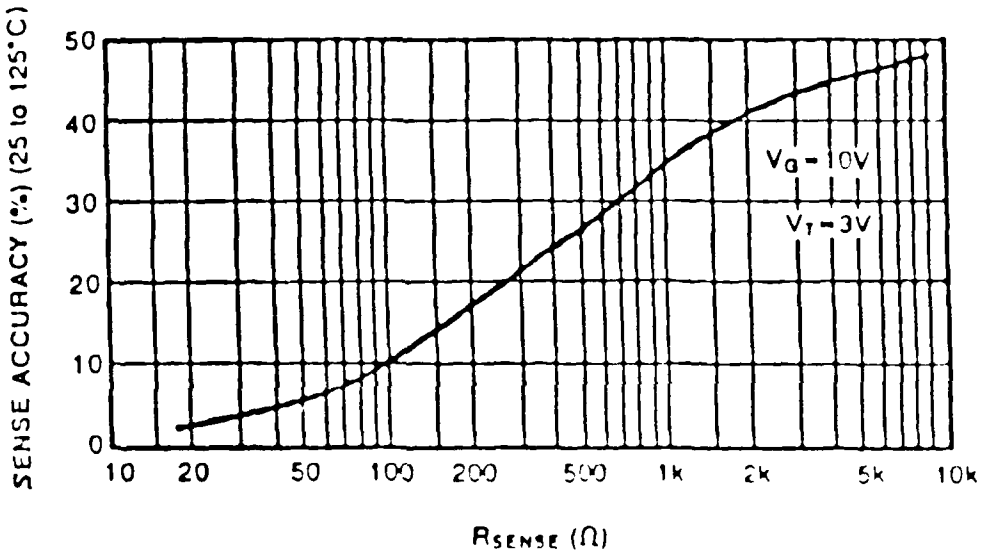

Figure 6: Thermal Accuracy of Sense Voltage (After Fay [9]).

for V_{Sense} may be seriously affected by noise. The CMFET does allow some accommodation for the reduction of noise in the sense voltage. Noise may be reduced by the use of what is called the "Kelvin" pin. This pin allows the bypassing of parasitic resistances and inductances from the package and the avoidance of ground loops [7]. This is accomplished by a direct connection to the load section source bonding pad, shown schematically in Figure 7. Therefore, for the greatest sense voltage accuracy, the sense resistor should be connected between the sense source pin and the Kelvin pin, as shown, rather than between the sense source pin and ground. At this point, it becomes convenient to introduce a new symbol for the CMFET that is easier to use. Figure 8 shows this new symbol, where the connection labeled by M is the sense-section source pin

The other consideration when dealing with small resistor values is whether or not a given resistor value will result in useful levels for the sense voltage. If the levels are not high enough, it becomes necessary to amplify the sense voltage. This introduces unwanted complexity into the circuit and a new source for errors in the output sense voltage. Noise and voltage level considerations will usually restrict the value of the sense resistor to between 10% and 100% of $r_{dm(on)}$[11].

This elegant method for developing a sense voltage proportional to the load current using the CMFET differs greatly from the more conventional method. Traditionally, such a voltage is achieved by placing a resistor directly in series with the load current, altering the operating conditions. The level of currents flowing through a resistor placed in such a position can be quite high, requiring the use of expensive wire-wound resistors [9,10,11]. In addition, such a resistor will dissipate significant amounts of power, on the order of watts. By contrast, using the CMFET allows the use of inexpensive resistors and results in power dissipation on the order of *milli*watts for the same situation [7] without affecting the load current at all. These factors, combined with the low cost of CMFETs [7], allow the user to perform the same function as before at lower cost and with power dissipation from the sensing function that is three orders of magnitude lower. Provided that the user is able to achieve sufficient accuracy from a CMFET circuit, this represents a

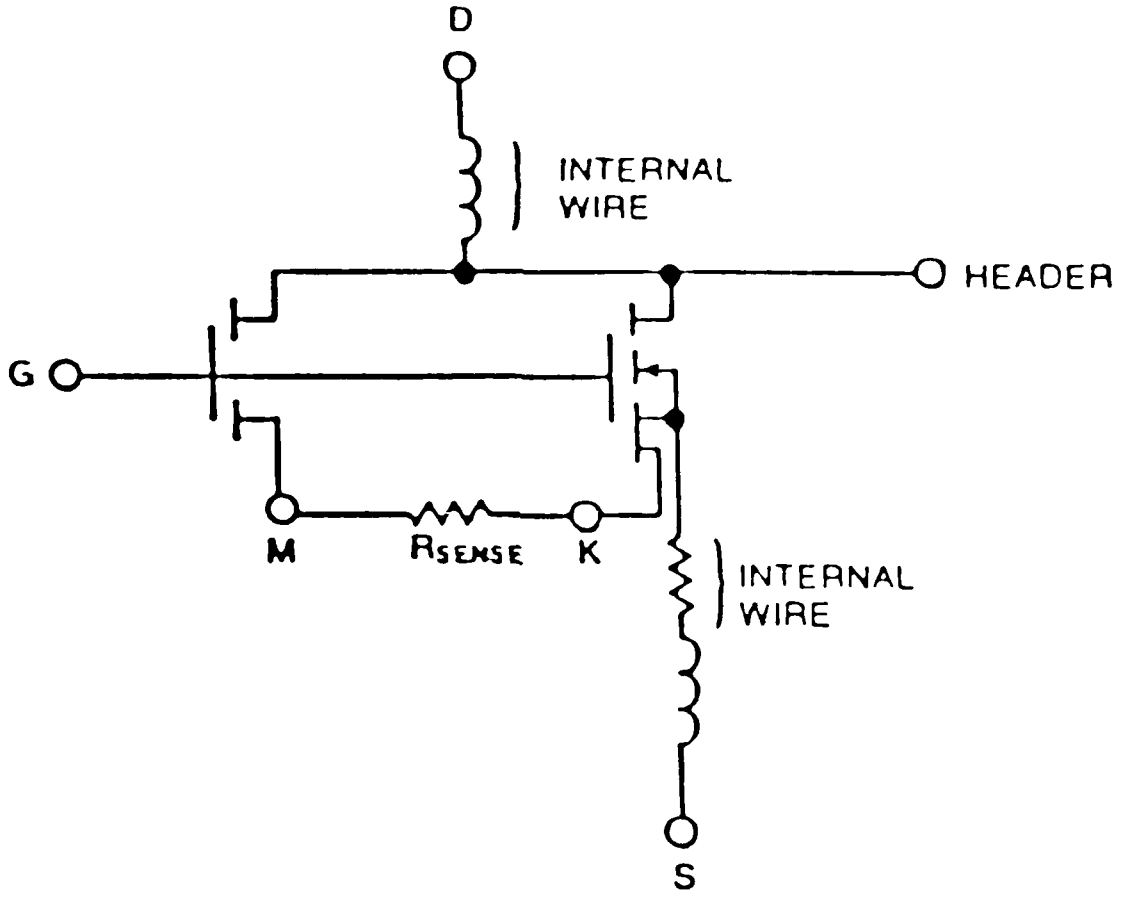

Figure 7: "K" marks the Kelvin Connection (After Fay [9]).

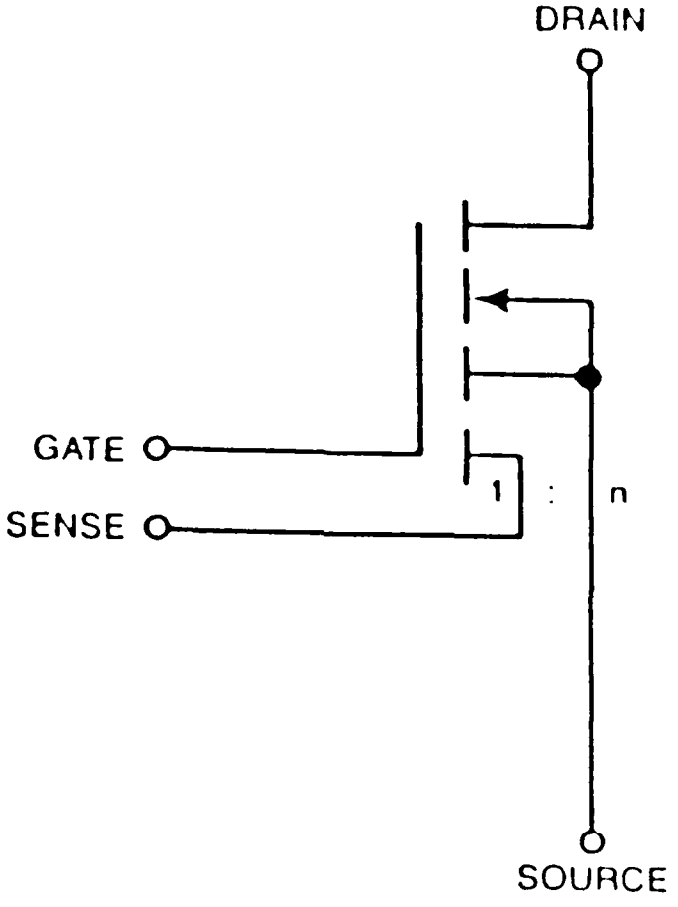

Figure 8: Five-terminal CMFET Symbol (After Schultz [8]).

significant advantage resulting from the use of the CMFET rather than the series power resistor method.

SECTION 1.4: BASIC RADIATION EFFECTS ON MOS DEVICES

When a semiconductor device is exposed to a radiation environment, its electrical properties and/or its operating condition are generally altered. Such alteration includes possibilities of degradation, upset, or failure. However, the nature and magnitude of the alteration depend on the specifics of both the environment and the device or circuit. Therefore, it is necessary to specify the type of radiation to be considered as well as the operating conditions of the circuit.

Radiation effects relevant to MOS devices may be placed in four broad categories: total dose effects, dose-rate effects, single event upset, and neutron effects. The first three are caused by ionizing radiation and the last by neutron exposure. Ionizing radiation includes both photons and charged particles. These may be grouped together since the net result of interactions of photons and charged particles is, qualitatively, basically the same. Through such interaction mechanisms as the photoelectric effect, Compton scattering, pair production, and Rutherford scattering, both photons and charged particles produce electron-hole pairs in quantities which depend on the energy of the incident radiation and the target material [12,13]. Generally, the only photons of sufficient energy and penetration to cause bulk ionization are photons in the x-ray and gamma-ray ranges. A secondary effect of ionizing radiation exposure of semiconductor materials is the displacement of atoms from their lattice positions. Normally, however, the dominant effect is that of ionization [14].

Ionizing radiation exposure is usually measured by the unit **r**adiation **a**bsorbed **d**ose or rad. A rad is equal to 100 ergs of energy deposited per gram of material. Because this varies from material to material, the particular material under consideration must be specified. Another measurement of ionizing radiation is the rate at which the energy is transferred. The ionizing dose rate ($\dot{\gamma}$) is normally expressed in rad/s.

The second general type of radiation, neutrons, has a very different effect than that of photons and charged particles. Because neutrons have no electric charge, they normally interact only with the atomic nuclei. Although these interactions include nuclear reactions, the dominant effect is the displacement of atoms from their lattice positions which produces defects in the lattice [15]. A secondary effect of neutron exposure is ionization due to the motion of displaced atoms. Once again, however, this secondary effect is strongly dominated by the primary effect of atomic displacement [15].

Neutron radiation is commonly measured in flux, particles per unit area per second, or fluence, total particles having passed through per unit area. However, since neutron interactions are strongly dependent on neutron energy [16,17], it is common to express neutron fluence in terms of a 1 MeV equivalent fluence. That is, fluence is expressed as the fluence of 1 MeV neutrons which would produce the same effect.

It should be apparent from the discussion above that in most cases ionizing radiation can be considered to create only electron-hole pairs through ionization and neutrons may be considered to cause only displacement damage. Unfortunately, neither of these gives any indication concerning the effects of radiation on the electrical properties of semiconductor devices.

Total dose radiation effects are those caused by long-term exposure to ionizing radiation delivered at a low dose-rate. These effects are important in MOS devices because of the presence of the silicon dioxide gate dielectric. This oxide typically contains large densities of charge trapping centers. Once carriers are generated through ionization, they tend to become trapped in the oxide, if they avoid initial recombination. The amount of initial recombination taking place is reduced as the electric field is increased, as when a gate bias is applied. This reduction in recombination is a result of the enhancement of the separation of charges by the electric field following their generation [18].

Thus, in the presence of ionizing radiation, charge accumulates in the gate oxide of MOS devices. The situation is further complicated by radiation-induced interface states at the silicon-silicon dioxide(Si SiO_2) interface. The creation of

these states is dispersive in time and can continue long after radiation exposure has ended [14,19]. Since, in operating n-channel devices, these traps manifest a negative charge, they contribute a positive threshold voltage shift whose magnitude depends on the silicon surface potential, because the potential will determine the occupancy of the interface states [20]. The net charge in the oxide is usually positive because the much higher mobility of electrons in the oxide allows them to be swept out of the oxide. At the same time, a positive gate bias (as is normal for n-channel devices such as the CMFET) will cause holes to move towards the Si-SiO_2 interface [21] where they may be captured in long-term trapping sites for periods which can last from hours to years [22]. This process is depicted in Figure 9.

It is known that such charges at the interface are undesirable because they represent a space-charge region which shifts the flatband voltage (therefore, the threshold voltage as well) [20]. The threshold shift following radiation exposure is generally time dependent. A typical time progression of threshold shift is shown in Figure 10. Because interface states may continue to be created and holes trapped in the oxide may recombine through tunneling, it is possible for the threshold voltage to shift positively with respect to the initial value following an original negative shift. This phenomenon is known as superrecovery or rebound [23,24]. Enough of a shift in the threshold voltage in either direction usually results in circuit failure. It should be noted that while threshold voltage shifts are not the only observed total dose effect, it is generally the one of major concern for MOS devices for most applications. The secondary total-dose effect which can be important is an increase in on-resistance, a manifestation of mobility degradation, caused by the interface traps acting as scattering centers.

The radiation effects of high dose-rate radiation exposure and single event upset are very different from total dose effects due to the magnitude of the radiation induced ionization. Dose rate ($\dot{\gamma}$) effects are caused by bulk ionization from exposure to a large ionizing radiation pulse (i.e., either electrons or photons). Single event upset (SEU) effects are caused by localized ionization from the passage of a single, energetic heavy ion. In either case, when this ionization occurs in the region of a biased junction (particularly a strongly reverse-biased junction), very

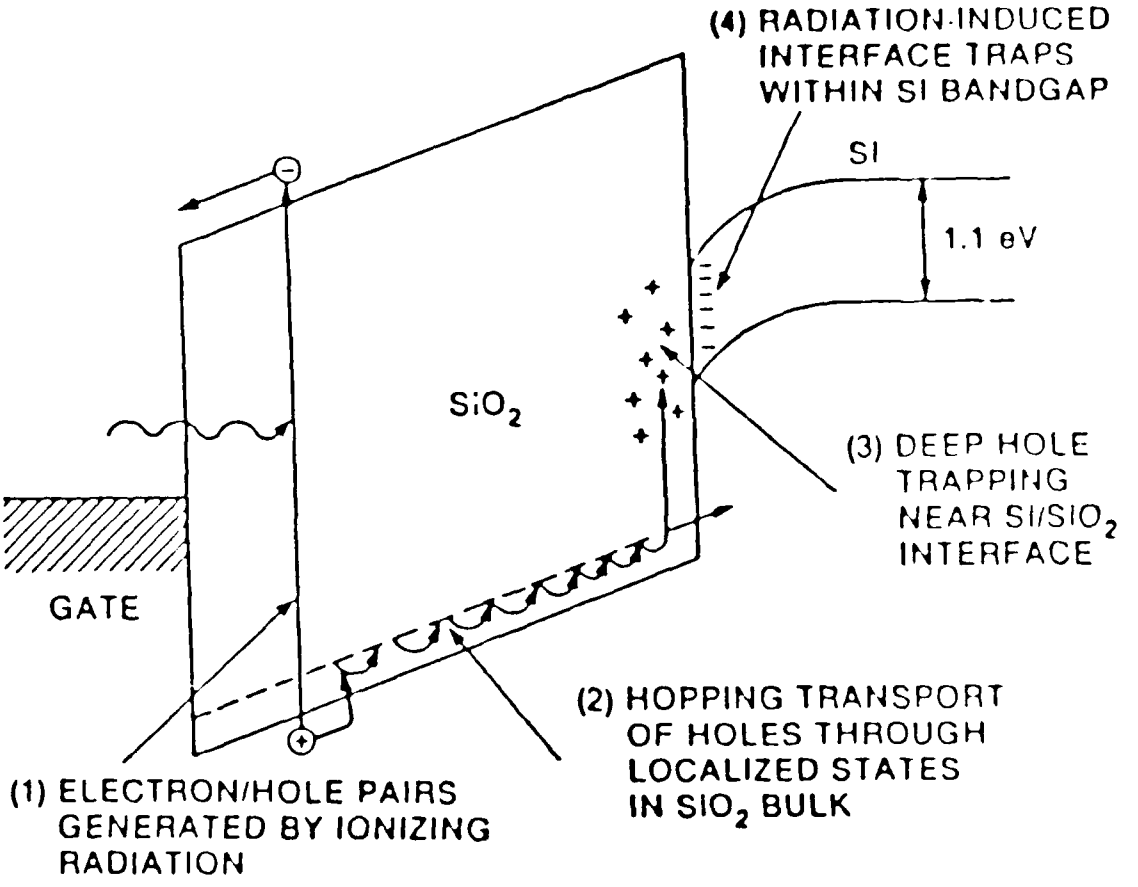

Figure 9: Schematic Total Dose Effects (After Mclean and Oldham [14])

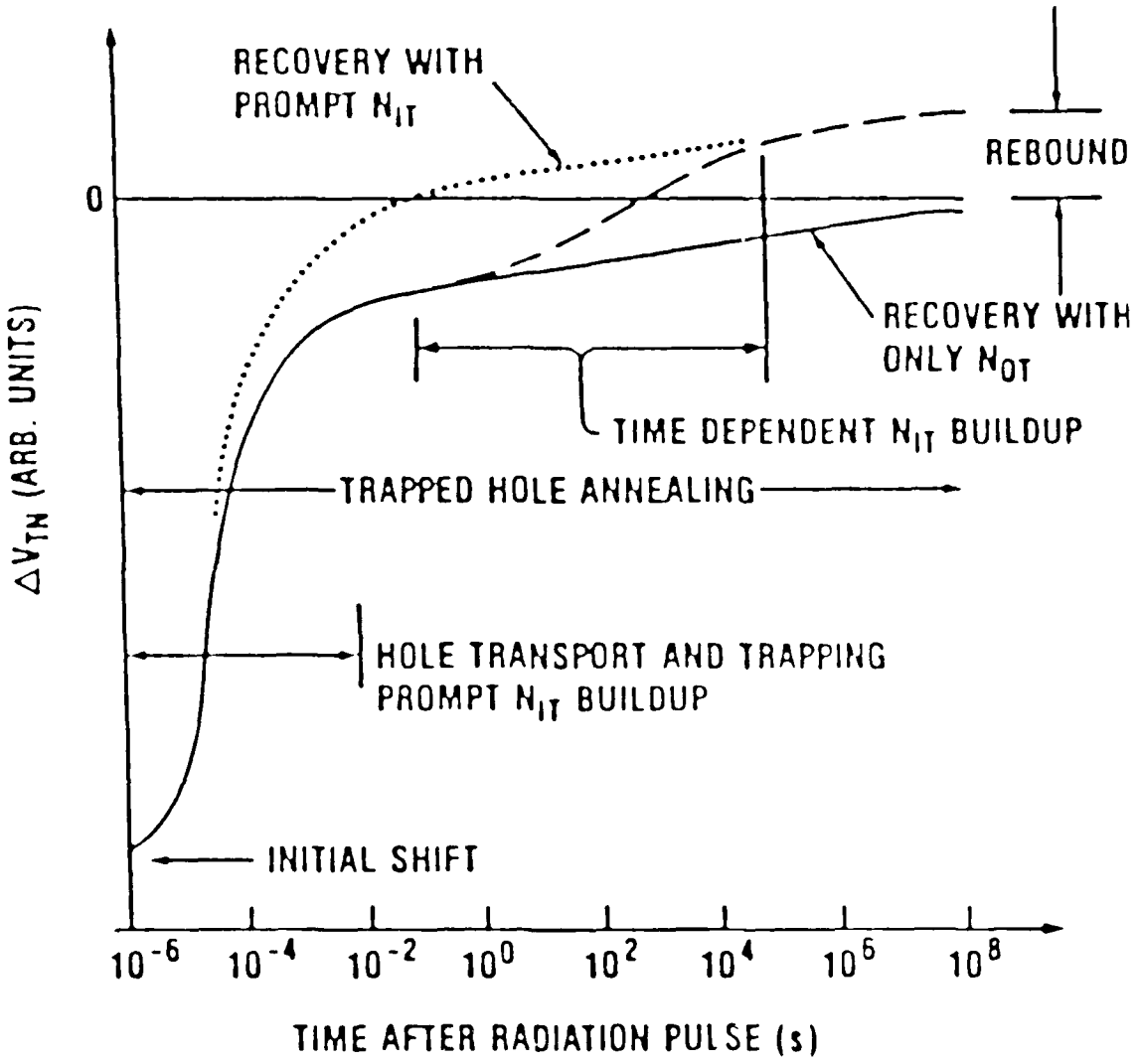

Figure 19: Time Dependence of Threshold Voltage (After Mclean and Oldham [14])

large currents result. These currents (in the $\dot{\gamma}$ case) are normally referred to as induced photocurrents. Such photocurrents can cause transient upset of circuits leading to such problems as latch-up [25] and damage to or failure of metal interconnects. Even if none of these occur, it is still possible to create errors in logic and memory devices which use stored charge to represent data [26]. These effects may be due to bulk ionization by $\dot{\gamma}$ or may be from localized ionization by the passage of a single energetic heavy ion. Dose-rate upset can be a major problem for DMOS power devices and can make power supplies which use them the weakest part of a system in a dose-rate environment [27].

All neutron effects are a result of displacement damage. Displacement damage in semiconductor devices affects their performance and characteristics in a manner very different from the ionizing radiation effects discussed above. The disruption of the periodicity of the lattice by the radiation-induced defects creates localized energy states within the band gap. Such states are known to enhance generation, recombination, tunneling, trapping, and compensation. In addition, the defects which created these states act as scattering centers which reduce bulk carrier mobility. However, such mobility degradation becomes significant only at high fluences. Nevertheless, because DMOS devices do not depend on minority carriers, the major effect of displacement damage is usually bulk mobility degradation, as seen through increases in on-resistance [1].

Since defects anneal to some extent, neutron damage effects are also time-dependent. However, annealing rates at room temperature are very small for times greater than 100 seconds [28]. Unless very long time periods are being considered, damage after this initial period may be considered to be approximately constant. Unfortunately, this does not simplify matters much since the amount of long-term damage caused by neutrons is dependent on many variables. These variables include neutron energy, target material type, resistivity (doping level), injection level, and temperature [14]. As a result, all these variables must be specified if there is to be any hope of accurately predicting the magnitude of displacement damage.

In the case of DMOS devices, then, it is possible to reduce expected radiation effects into four primary effects. Total ionizing dose exposure causes threshold voltages to shift and the channel mobility to degrade, $\dot{\gamma}$ can cause transient upsets and damage including burnout, energetic heavy ions can cause more localized transient upsets known as SEUs or single event burnout (SEB), and neutron exposure can cause increases in on-resistance at high fluence levels.

CHAPTER 2: FIRST-ORDER ANALYSIS AND PREDICTION OF RADIATION RESPONSE OF CMFETs

SECTION 2.1: GENERAL RESPONSE OF CMFETs TO RADIATION EXPOSURE

As was previously mentioned, the sense voltage created by using a CMFET is potentially useful in circuit control. An example of such an application will serve to demonstrate the potential for using devices like the CMFET in radiation environments. Figure 11 shows an example of using a CMFET in feedback control through a pulse width modulator (PWM), where the CMFET itself is inside the dotted lines. The PWM in this case is simply a gate biasing device which is controlled by the voltage comparator. In such a circuit, the PWM gate drive is disabled whenever the sense voltage becomes equal to or greater than the reference voltage. This will maintain an almost constant load current provided that the current ratio $n' = I_L/I_S$ remains constant with time and changing conditions. If the user is free to choose the value of the reference voltage, it may be chosen to minimize the necessary sense voltage and sense resistor value so as to maximize the accuracy of the current ratio. However, if the reference voltage is fixed by other circuit considerations, the user is restricted to using the sense resistor value which corresponds to equal sense and reference voltages for the desired load current.

The potential advantage that might be derived from such an application of the CMFET is a direct consequence of the feedback control aspect of the circuit. If the effects of radiation on other parts of the circuit are ignored or assumed to be made up of device types which are not affected by the type of radiation being considered, it is apparent that if n' does not change significantly under changing conditions induced by radiation, then the feedback control may prolong the circuit life far beyond what it would be without the control. For example, a CMFET circuit which maintains a reasonably constant n' could theoretically keep the load current constant for as long as the threshold voltage remains positive. Failure for an uncontrolled device can be defined as a threshold voltage shift of 0.5 V (typical for most MOSFETs but small for power MOSFETs, as will be shown). Using this definition and assuming an original threshold voltage of 3.5 V (an actual

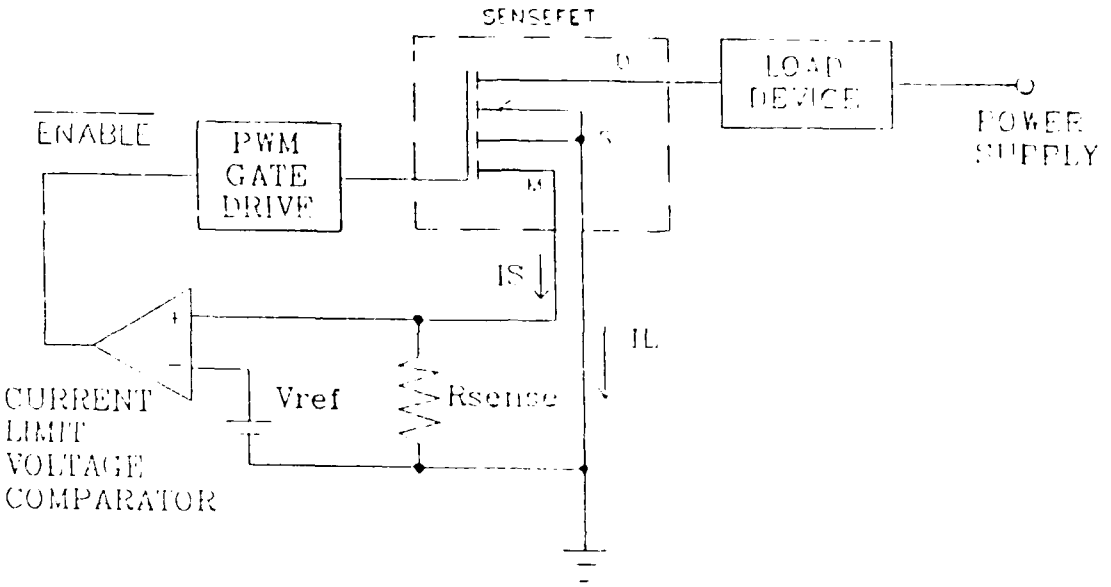

Figure 11: Feedback Control Using a SMFET (After Schultz [11]).

measured value), this feedback control concept allows a tolerable shift which is seven times greater than that without the feedback circuit. Naturally, any such feedback circuit would accomplish as much, but it is the CMFET which makes this approach practical.

This potential increase in circuit lifetime hinges principally on maintaining a certain level of accuracy in n' while phenomena such as shifting threshold voltages and increasing on-resistance take place. Therefore, it is desirable to make some first-order calculations to see if this is a reasonable expectation.

A reasonable starting point is consideration of total ionizing dose effects: that is, the effects of threshold voltage shifts on n'. In terms of circuit operation, a negatively shifting threshold voltage means that the PWM would drive the CMFET gate for shorter periods of time. Provided that the cycling time through the feedback loop is fast enough and n' does not change appreciably, the circuit should maintain its near-constant load current. Although using a PWM as a gate driver actually represents a *transient switching condition*, calculation of d.c. current ratios still should give an indication of the effectiveness of the circuit under radiation-induced changes.

To examine this situation, the basic square-law model must be re-examined. Because only a first-order result is sought, some simplifying assumptions will be made. First, it is assumed that the CMFET always remains in the linear region of operation. It will also be assumed that the radiation-induced changes in threshold voltages will be slow and will be approximately constant over short periods of time. Neither of these are unreasonable assumptions and actually do apply in a number of interesting situations. In particular, the assumption of slow changes in threshold voltages corresponds to a space environment. In addition, the gate and drain voltages will be treated as constant values and only the threshold voltages will be allowed to vary, all of which is realistic for the PWM example circuit. Having made these assumptions, it is possible to carry out a simple analysis.

By simply inserting a new term for the threshold voltage shift, ΔV_{TL} the new d.c. load current is given by

$$I_L = 2K_L[(V_{G1} - V_{TL} - \Delta V_{TL})(V_{DS1}) - \frac{1}{2}V_{DS1}{}^2]. \tag{9}$$

Similarly, the new d.c. sense current is given by

$$I_S = 2K_S[(V_{G1} - V_{TS} - \Delta V_{TS} - V_{Sense})(V_{DS1} - V_{Sense}) - \frac{1}{2}(V_{DS1} - V_{Sense})^2]. \tag{10}$$

However, V_{Sense} will also change when I_S changes since

$$V_{Sense} = I_S R_{Sense}. \tag{11}$$

where R_{Sense} has a value that is fixed by (7) and (8) for V_T equal to the initial threshold voltage. Thus,

$$\begin{aligned} I_S = 2K_S[&(V_{G1} - V_{TS} - \Delta V_{TS} - I_S R_{Sense})(V_{DS1} - I_S R_{Sense}) \\ &- \frac{1}{2}(V_{DS1} - I_S R_{Sense})^2]. \end{aligned} \tag{12}$$

Solutions to this equation are best found iteratively. By solving these current equations for particular threshold shifts, the resulting current ratio is found easily from $n' = I_L/I_S$ for the combination of V_{TL} and V_{TS} of interest. The possibility of asymmetric shifting in the threshold voltages is allowed because of the different gate biasing levels seen by the load and sense gates. (Although any asymmetry would be expected to take the form of a more rapidly shifting load threshold, the opposite case is also included for completeness.) As will be shown, such asymmetry is to be avoided. Avoiding asymmetry means that V_{Sense} should be made as small as possible. Because this is desirable for other reasons as well, this condition presents no great obstacle.

These results are only meaningful when compared to some kind of control condition. A common specification for failure due to threshold voltage shifts in non-power applications is a shift of 0.5 V. Without the feedback loop, a negative

shift of this magnitude corresponds to an increase in I_L of 8.6%. Therefore, only shifts in n' greater than 8.6% will be considered to be circuit failures*.

Looking at Table 1 shows that for $\Delta V_{TL} = \Delta V_{TS}$, failure occurs for a threshold shift of approximately 1.75 V. (Parameters used in this example calculation are given in Table 1.) This is almost a four-fold increase in tolerable shift for the circuit as a whole. Table 1 also shows that, if V_{TL} shifts faster than V_{TS}, failure is reached much more quickly, so this situation must be avoided whenever possible.

The effect of using a smaller sense resistor value is shown in Table 2. Here $R_{Sense} = 70\ \Omega$, corresponding to a $V_{Sense} = 0.63$ V for $I_L = 10$ A. The shift in n' for $\Delta V_{TL} = \Delta V_{TS}$ is appreciably smaller in this case. The results in Table 2 would seem to imply that circuit failure would not occur until V_{TL} becomes zero. Additionally, the smaller resistor value implies a smaller chance of asymmetric threshold shifting.

Such a situation is promising particularly in the case of a higher initial threshold voltage. If the initial value is 3.5 V (an actual measured value for this device) and if a small enough resistor value can be used to keep n' from shifting more than 8.6%, then it may be possible to increase the useful circuit life by seven times over the life of a circuit without the feedback loop made practical by the CMFET. Such favorable indications provide the impetus to examine this situation more closely. It is possible that not only may this particular circuit have increased radiation hardness at relatively little expense, but that the concept itself could be applied to many other situations.

While the analysis above appears to yield promising results, the operating conditions which were chosen represent something of an extreme with respect to the typical operating conditions for power devices. In most applications, such as switch-mode power supplies, the power device is switched at a high frequency and the "on" state is typically well within the linear region ($V_{GS} - V_T \ll V_{DS}$). This means that as long as the threshold voltage allows the device to be turned completely

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* For this analysis, values such as K_L, K_S, V_T, and V_{DS} were taken from or calculated from early-release data sheet information for the MTP10N25M CMFET. They may not necessarily represent measured values.

Table 1: Percent current ratio shift for various threshold voltage shifts. Parameters as shown.

ΔV_{TL} (V) \ ΔV_{TS} (V)	0	−0.5	−1.0	−1.5	−2.0
0	0	−5.8	−10	−15	−19
−0.5	8.6	2.4	−2.9	−7.5	−12
−1.0	17	10	4.7	−0.2	−4.5
−1.5	26	19	13	7.2	2.6
−2.0	34	27	20	15	9.6

V_{sense} = 1 V @ I_L = 10 A R_{sense} = 131.8 ohms

V_{GS1} = 10 V V_{DS1} = 3.4 V $V_{TS} = V_{TL}$ = 2.5 V

K_L = 253.55E−3 A/V^2 K_S = 298.29E−6 A/V^2

Table 2: Current ratio shift for a smaller sense resistor value.

ΔVT (V)	n'	$\Delta\%n'$
0	1105	-
-0.5	1122	1.54
-1	1139	3.08
-1.5	1156	4.62
-2	1173	6.15
-2.25	1181	6.88

on and off, the magnitude of the threshold voltage does not affect device operation significantly. In other words, the threshold voltage may shift negatively until it is equal to the low gate-to-source bias level or positively until $V_{GS} - V_T$ and V_{DS} are of the same order of magnitude at the high gate-to-source bias level without having much effect on the performance of the device in the circuit.

Such a situation may seem good at first glance, but it should be noted that the rate of threshold voltage shift is a strong function of oxide thickness [18]. Therefore, while most power MOSFET circuits can tolerate large shifts in threshold voltage, the thicker gate oxides necessary for power MOSFETs result in a significantly more rapid failure from threshold shift than for many ordinary MOSFETs with very thin gate oxides [29]. However, as noted earlier, CMFET-type devices may still be desirable for use in radiation environments because of the benefits that they can provide which are not related to radiation response.

Thus, it is important to be able to apply results concerning the radiation response of the current ratio to CMFET use in other applications. This is a very straightforward problem since the requirement for current-ratio stability is the same as for the hardening concept above. Although the required accuracy will be dependent on the application, it is important to know what the limitations of such devices are with respect to radiation exposure.

The next situation of interest is that of increasing on-resistance from a neutron fluence. Examination of the situation reveals it to be directly analogous to a changing n' from thermal excursions. Therefore, it is useful to use the same on-resistance model that was used in that case (Figure 5). Once again both on-resistances should change by the same factor since the conditions pertinent to neutron displacement damage, such as resistivity, temperature, and injection level should be very nearly identical throughout the entire CMFET. For most types of resistors, the resistance will not change in the same manner as the on-resistances, so the ratio n' must change. Using the on-resistance model allows a simple calculation of the possible magnitude of changes in n'.

The model [11] shows that n' may be found simply to be

$$n' = \frac{r_{dm(on)} + R_{Sense}}{r_{ds(on)}}. \tag{13}$$

Since, as stated earlier, R_{Sense} is normally 10% to 100% of $r_{dm(on)}$, for a large increase in on-resistances n' becomes approximately

$$n' = \frac{r_{dm(on)}}{r_{ds(on)}} \tag{14}$$

if R_{Sense} remains constant. However, $r_{dm(on)} = nr_{ds(on)}$, so n' approaches n for large increases in on-resistance. Therefore the larger the initial current ratios, the larger the possible change in the ratio from neutron bombardment. Since the initial n' is larger for larger sense resistor values, once again there is a motivation for making R_{Sense} as small as is tolerable. The results from using the simple technique outlined above are shown in Table 3. Clearly, such shifts in the current ratio are not tolerable, yet there may be a way around this problem in some situations.

The on-resistance model shows that if R_{Sense} were to change at the same rate as the on-resistances in the CMFET, then the current ratio would remain constant. In order to accomplish this, the materials and conditions found in the CMFET must be matched as closely as possible. An approximate match is found in a semiconductor resistor of the same resistivity as the n-epi drain region. Unfortunately, a constant n' and an increasing R_{Sense} also means an increase in V_{Sense} at any given load current. However, for a large enough initial R_{Sense}, increasing this resistance has little effect on V_{Sense} as shown in Figure 12. Thus, the user is faced with a trade-off between accuracy in a high-neutron fluence environment and accuracy in linearity and thermal excursions. Nevertheless, it is quite possible that situations may exist in which changes from neutron effects are the most important consideration.

It is useful now to consider how this compares to using an ordinary power MOSFET and a series power resistor for current sensing. In such a situation, the sensing voltage would not lose any accuracy from a neutron fluence unless

Table 3: The dependence of current ratio shift on sense resistance in a neutron environment.

R_{Sense} (Ω)	$\Delta\%n'_{max}$
131.8	-35.5
70	-23.1

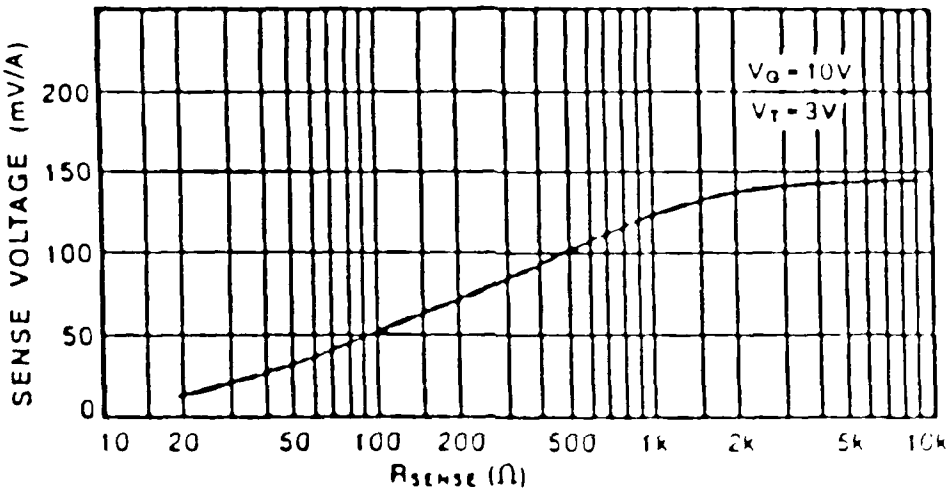


Figure 12: Vsense approaches a limiting value for large Rsense (After Fay [9])

displacement damage in the wire windings of the resistor was enough to increase its resistance, which is unlikely.

Next, transient radiation effects on the CMFET will be addressed. As far as hardening against SEU effects is concerned, no advantage is to be expected from the use of a CMFET. If the CMFET actually monitored load current rather than simply mirroring it, hardening might be possible. Since this is not the case, a heavy ion could actually disrupt a significant portion of the load section without a noticeable effect on the sense section. In fact, CMFET schemes may be worse than other sensing schemes since they would be less likely to detect such an upset.

There is, nevertheless, hope for better performance in the case of $\dot{\gamma}$. Since $\dot{\gamma}$ affects the entire device the effects on the load section would be reflected in the sense section as well. This allows the use of the sense voltage as a detector for $\dot{\gamma}$; particularly if the sensing cells are intentionally made more sensitive to such pulses so that protection would always occur before the load section could be upset. For example, a sufficiently large sense voltage indicating radiation-induced photocurrents and resulting breakdown could trigger the interruption of the drain-source voltage for a long enough time to allow most of the excess carriers to recombine. Thus, if the circuit could withstand such an interruption, it would be effectively immune to the deleterious effects of $\dot{\gamma}$. This is important because, without protection, the sensitivity of DMOS power devices to dose-rate upset and the large reverse voltages seen by such devices usually forces the designer to derate the maximum allowable reverse bias severely, necessitating the use of devices with much higher voltage ratings. These high voltage devices are typically more expensive and may have higher on-resistance.

Although the CMFET is at best no better than ordinary MOSFETs for SEU and neutron fluence situations, there is substantial promise for the other situations. CMFETs show a possibility for providing an advantage in total ionizing dose situations in certain special cases and for being at least as good as normal power MOSFETs in most other application circuits. Also, CMFETs show great promise for use as a $\dot{\gamma}$ detector to provide upset protection for the power circuit.

SECTION 2.2: ANALYSIS OF RESPONSE TO TOTAL-DOSE EXPOSURE DURING LINEAR OPERATION

At this point, the results that would be expected for total dose exposure based on the qualitative behavior of the first-order MOSFET model will be discussed. Since the effects of asymmetric shifting of the threshold voltages have already been discussed in the previous section they will not be repeated here.

The linear region of operation will be examined first. Since any changes in n' would have to be a consequence of the differences in the form of the current-voltage responses of the load and sense sections, as they are used in a circuit, this response gives insight as to how n' should change with exposure to ionizing radiation.

It has already been noted that the presence of a non-zero sense voltage will degrade the linearity of n', and it is precisely this degradation which should explain any shifts in n' due to threshold voltage shifts. More specifically, if the load and sense sections of the device respond differently to changes in voltages applied to the circuit, it is quite reasonable to expect that n' will shift if these voltages change. The question, then, is what should be the magnitude and direction of the shifts?

The direction of shifts is shown simply by examining the relative differences in behavior of the load and sense sections. In the linear region of operation, the presence of a sense resistor gives the I_D versus V_{DS} plot for the sense section a different shape from that of the same plot for the load section. (The actual experiment will be anticipated here by assuming that there is non-negligible parasitic resistance in the source lead of the load section.) If the sense and parasitic voltages are equal, then the plot for the sense section will simply be the plot for the load section scaled down by the factor n, meaning that the current ratio will be invariant with respect to V_{DS}. However, this is a trivial case. If the sense voltage is greater than the parasitic voltages in the load leads, the plot will be more linear than that for the load section over the same range of V_{DS}. In other words, line sense current is no longer an exactly scaled version of the load current. If the sense voltage is smaller, the plot for the sense section will be less linear than the plot for the load section.

Therefore, in the case of sense voltage being greater, if V_{DS1} is decreased, the load current will decrease more slowly than the sense current times the original

n' and n' will increase. For the case of parasitic voltage being the greater of the two, if V_{DS1} is decreased, the load current will decrease more quickly than the sense current times the initial n', so n' will decrease.

To relate this to radiation effects, the qualitative changes in the plot of I_D versus V_{DS1} must be considered when threshold voltage shifts negatively and V_{GS1} is held constant. If V_{DS1} is also held constant or decreased (for a constant load current), the operating point for both the sense and load sections changes such that it is at a smaller V_{DS1}, relative to that needed for saturation, than it was prior to irradiation. Qualitatively, then, this is very similar to merely decreasing V_{DS1}. Therefore, it is to be expected that under the testing conditions, if effects on K_S and K_L are ignored, there will be a downward shift of n' if V_{Sense} is less than the parasitic voltage and upward if V_{Sense} is the greater of the two.

While the non-idealities of real devices make a precise quantitative analysis unwieldy, it is possible to make a few observations about the relative magnitudes of any expected shifts. When $V_{GS1} - V_T \gg V_{DS1}$, the operating points are already far from the saturation point and reducing the threshold voltage does not change this relative position much. It is expected, then, that very small shifts in n' would take place for this condition, even for large sense voltages. In addition, as was noted earlier, non-linearity in n' is minimized for small sense voltages. Therefore, the largest changes should be for large sense voltages and an initial operating point near saturation, and the smallest changes should be for small sense voltages and starting with $V_{GS1} - V_T \gg V_{DS1}$.

SECTION 2.3: ANALYSIS OF RESPONSE TO TOTAL-DOSE EXPOSURE DURING SATURATION OPERATION

The other operating condition of interest is that of deep saturation, that is, $V_{GS1} - V_T \ll V_{DS1}$. Analysis of this situation is much simpler since there is almost no dependence on V_{DS1}. The current in each section is dependent simply upon the square of the gate voltage minus the quantity of the threshold voltage plus the sense or parasitic voltage, as applicable. Therefore, unless the parasitic and sense

voltages are always equal, n' must change as threshold voltage shifts, especially when those voltages are, themselves, dependent on the currents which are functions of the threshold voltage (for non-constant current situations).

It is easily shown that if V_{Sense} is consistently larger than the parasitic voltage and the difference between them does not decrease, n' must increase, since the load current rises more rapidly. Conversely, if V_{Sense} is smaller and does not become larger than the parasitic voltage, then n' must decrease since the sense current would then be the one increasing more rapidly.

It should be expected that shifts in n' will be larger for operation in saturation than for linear operation since there is a squared dependence on the terms affecting the shift rather than a linear one. Again the shifts should be minimized for sense voltages which do not differ much from the parasitic voltages (or for small sense voltages if parasitics are not present). Because of the high currents associated with saturation operation of power MOSFETs, only relatively low gate biases are normally used, so the dependence of shifts in n' on this voltage will not be discussed.

The descriptions of DMOS devices, CMFET operation, and basic radiation effects allow one to examine the effects of radiation environments on CMFETs. A first-order examination indicates that significant radiation hardening may be achieved through judicious circuit application of the CMFET. The possibility of very small changes in the current ratio n', especially for linear operation, is also predicted. Yet, while all this looks quite promising, it is only by experimental verification through exposure to radiation environments that firm conclusions may be reached. It is shown in this work that such experiments confirm the first-order predictions.

CHAPTER 3: SETUP AND EXPERIMENTAL PROCEDURE

The analysis of Chapter 2 was verified through experimentation. The focus of the experiments was not on the PWM circuit shown in Figure 11, but on the d.c. circuit of Figure 13. The latter circuit was judged to be more likely to yield information on the basic radiation response of the CMFET itself in a clear fashion because of the absence of control circuitry. Additionally, only total ionizing dose testing and limited $\dot{\gamma}$ testing proved to be practical for the scope of this work.

Although it would be preferable to use an equivalent circuit SPICE simulation for second-order predictions before proceeding with an experiment, such a simulation was not possible for the CMFET. SPICE simulation was not possible because of the unavailability of many of the important parameters necessary for a level 2 simulation. Therefore, it was necessary to begin experimentation without the benefit of further simulation.

The circuit in Figure 13 shows the actual circuit used and the external connections that were employed. During irradiation, the circuit was operated with the relays closed. Biasing was provided by a BK 1630 power supply supplying a gate biasing voltage and by a Hewlett-Packard 6023A autoranging power supply for the drain to source biasing voltage. Sense voltage was read using a Fluke 77 digital multi-meter (DMM) connected to the mirror terminal. The load current, I_L, was measured using the current-monitor terminals of the 6023A read by another Fluke DMM. To allow easy interchange of the CMFET devices, the CMFET was placed in a socket after bending the device pins into the proper configuration. For the sense resistor, a 1 kΩ, ten-turn potentiometer was used. The parasitic resistances shown are the result of the long (approximately 20 ft.) lines necessary for remotely biasing the circuit while in place in the Co^{60} irradiation facility. (All lines longer than a few inches were coaxial cable with shielding grounded at both ends.) Because of the parasitics and the voltage drops associated with them, separate grounds were used for the load and sense currents.

It should be noted that because of the heat dissipation large enough to damage the CMFET (junction temperature > 150 Celcius), it was necessary to

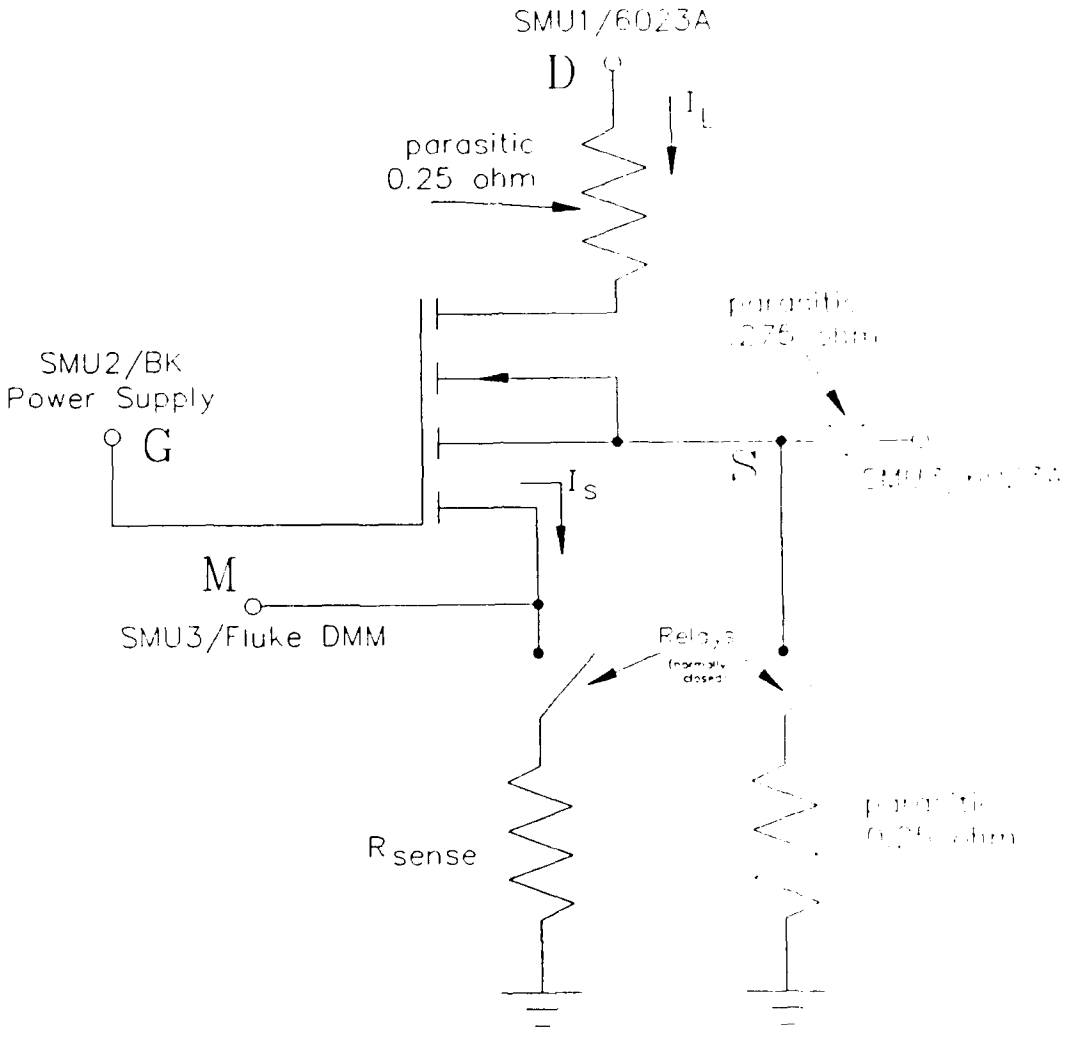


Figure 13: CMFET D.C. Test Circuit

mount the package on an anodized aluminum heat sink and use a fan to remove the heat. Even after taking these precautions, it was not possible to operate the device in a steady state at currents greater that 3.5 A without risking damage to the device from overheating.

Following each irradiation, threshold voltages and I_{DS} versus V_{DS} measurements were made using a Hewlett Packard 4145B semiconductor parameter analyzer. For these measurements, the relays were opened. The sense and load portions of each device were tested separately , using the appropriate terminals and the stimulus and measurement unit (SMU) connections shown in Figure 13. Because of the large currents typical of the load portion of CMFETs, the 4145B alone was not sufficient. It was, therefore, necessary to remotely operate the 6023A supply through its voltage program and current monitor terminals. Operating in this mode, the supply will output a voltage four times larger than the input program voltage and will show a current monitor voltage with one-sixth the magnitude of the output current. Voltage programming and current monitoring were accomplished via SMU1 and SMU3, respectively, of the parameter analyzer. This method was found to provide accurate results through comparison to direct biasing and measurement.

To measure the threshold voltages, the square-root of the drain current was plotted against the gate-to-source voltage with a sufficiently high (e.g. 10 V) drain-to-source voltage to assure operation in the saturation region. The two points nearest the point of maximum slope were then used to perform a straight-line extrapolation to the x-axis intercept to yield a threshold voltage. [It was important when measuring the threshold voltages for the load section to include the voltage drop due to the parasitic resistance of the source line (0.275 Ω).] From the same plot, the constants K_L and K_S were extracted by simply squaring the slope of the same extrapolation line. Sample parameter analyzer programs are shown in the Appendix.

Two current-ratio measurements were made for each set of measurements. The first was the measurement of n'. This was accomplished in a very straightforward manner. The load current was divided by the sense current found from the

measured values of R_{Sense} and V_{Sense}. Finding the intrinsic current ratio of the device, n, was not so simple.

Although the manufacturer measures the intrinsic ratio under a specific set of biases regardless of how the device is actually used, this was judged to have limited merit for typical applications. A more meaningful measurement uses the load and sense currents which result when biasing is at the same levels as during operation, but with the mirror terminal returned to ground directly rather than through a sense resistor. The intrinsic ratio which was measured was only about half that which was published by the manufacturer, even when measured in the same way, because the large parasitic voltage drops reduced the resulting load current.

While it is felt that the measurement methods used were sufficiently accurate, it is wise to include an estimate of the errors inherent to the measurements. Comparison testing showed threshold voltage measurements were in error by a maximum of ± 0.05 V from noise and ground level fluctuations. The corresponding errors in K_L and K_S were found to be about $\pm 2\%$, for the same reasons. Sense voltage measurements were found to vary less than 8 mV from the actual values at the sense section source due to parasitic drops and ground potential fluctuations. The load current measurement accuracy was within 10 mA, giving a current ratio measurement accurate to within about 1.5% of the actual value. Although these error estimates are not the result of exhaustive analysis, they represent the proper order of magnitude necessary to justify confidence in the measurements used for analysis.

The test circuit was irradiated in the Co^{60} gamma ray irradiation facility operated by the Department of Nuclear and Energy Engineering at the University of Arizona. The die were perpendicular to the gamma beam. This facility contains a Co^{60} source with an activity of about 200 Curies mounted to provide a beam of gamma radiation in a cavity with the approximate dimensions $12 \times 14 \times 36$ inches. The dose rate used was approximately 166 rad(Si)/s and was calculated from a formula based on the inverse-square relationship between dose rate and distance from the source, which has been calibrated through measurements performed through the National Bureau of Standards. Measurements were taken at intervals such that the shift in threshold voltage was relatively small between measurements (less than

0.25 V), and they were taken while the circuit was shielded from the radiation source.

By the methods outlined above, shifts in n' were tabulated as a function of threshold voltage shift as well as a function of total ionizing dose. This procedure was performed twice for most distinct sets of circuit conditions and once for some of the saturation cases since there was a limited supply of test devices and these cases were deemed least important. Circuit conditions were varied by providing different values of sense resistance and by changing initial biasing voltages to set the region of operation (i.e., linear or saturated). In terms of relative values of sense resistance, 20 Ω was judged to be a representative low value, 100 Ω a moderate value, and 1000 Ω a very high value. However, some other values were used in order to produce sense voltages that differed from the load source potential by a reasonable margin (about 100 mV) to compensate for the parasitic voltage drop. In some cases, voltages were held constant throughout the irradiation and the current was allowed to change. In other cases, load current was held constant with changing drain-to-source voltage or gate-to-source voltage, as appropriate, to simulate the current level of a constant-current feedback situation.

After collecting this basic data, the circuit of Figure 14 (similar in concept to the PWM circuit) was used to demonstrate the principle of adaptive control for compensation of radiation-induced effects. For this circuit, an operational amplifier (LF357A) was used to bias the gate of the CMFET. The goal of this circuit is to adjust the gate drive for a CMFET which is in saturation so that compensation will be made for shifts in threshold voltage. The output of this op-amp is simply the difference between the reference voltage, V_{ref}, and the sense voltage, V_{Sense}, multiplied by the closed-loop gain of the op-amp, where $V_{ref}$is given by a 25 kΩ potentiometer biased by a 1.5 V battery. The closed-loop gain of the op-amp is approximately $\frac{R_2}{R_1}$. When the gate isolation resistor, R_{iso}, is of a sufficiently high value, the circuit will not oscillate, but instead will simply stay at a stable operating point determined by R_1, R_2, V_{ref}, and R_{Sense}. C_1 and C_2 are used to filter noise and have the values of 0.33 μF and 10 μF respectively.

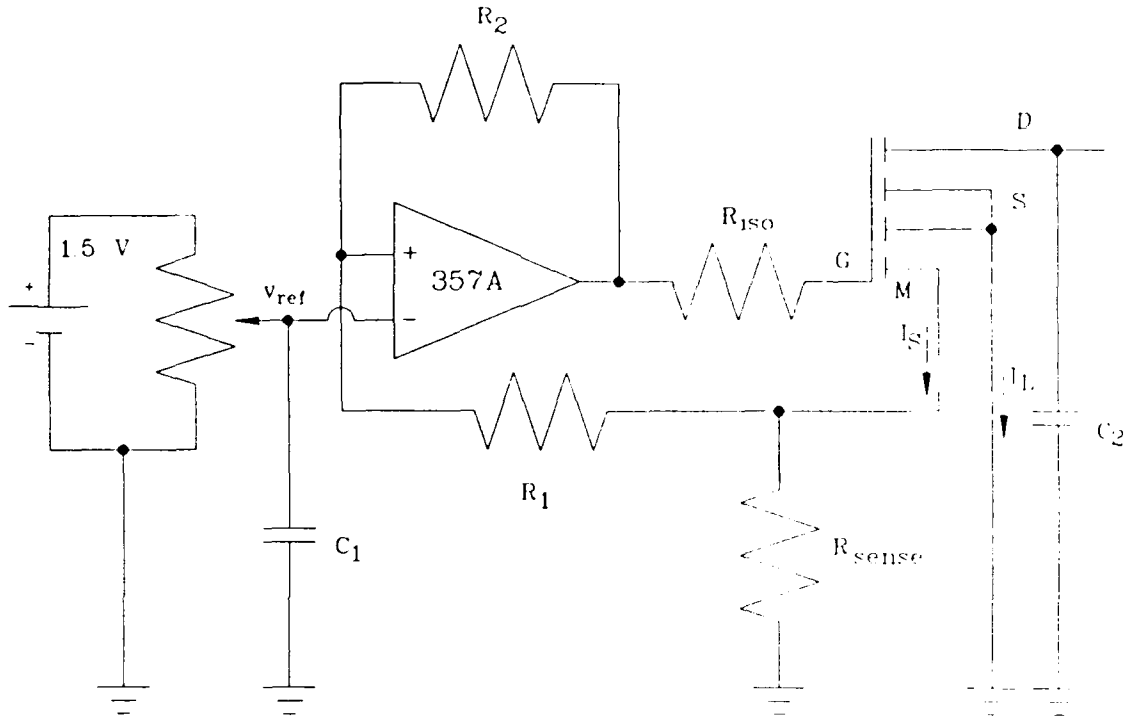


Figure 14: Operational-Amplifier Circuit

To test this circuit, the CMFET was irradiated under a constant gate bias and periodically removed and placed in the op-amp circuit to measure changes, after the threshold voltages were measured in the same manner as before. To monitor changes in the performance of the op-amp circuit, load current was again measured using the current monitor voltage of the 6023A and V_{ref}, V_{Sense}, and the output voltage of the op-amp were measured with a Fluke DMM. This procedure was followed for different values of closed-loop gain, sense resistance, and reference voltage.

CHAPTER 4: RESULTS FROM TOTAL DOSE EXPERIMENTS

The results from the total-dose experiments were very encouraging, showing that CMFETs can be used in total-dose environments under certain conditions. There were, however, difficulties in interpreting the results which should be considered before the results themselves are discussed.

The principle difficulties involved in analyzing the response of the devices to total ionizing radiation dose were parasitics in the circuit and non-idealities in the device itself. Parasitics were a problem because of the high currents being used. Such high currents resulted in voltage drops on the drain and source lead that were on the order of one volt. The reason that this was problematic was that the source potential of the load section was not a constant, as the ideal equations used previously assumed, which drastically altered the current ratio. This effect tended to obscure the radiation effects on the ratio if the current level in the load section was allowed to change.

The parasitic effects were dealt with by keeping the load current constant by changing V_{DS1} (or V_{GS1} if operating in saturation). By keeping the load current constant in this manner, it was possible to better distinguish radiation effects from parasitic effects.

The non-idealities mentioned above refer to a departure from the behavior predicted by the simple square-law equations used for the first order calculations. Although such a departure was not unexpected, it made the analysis of the radiation effects more complicated. There were two primary non-idealities. The first was saturation at a higher drain-source voltage than the simple model predicts. The other effect was lower than expected saturation current. Combined, these two effects resulted in lower than expected currents in the linear region of operation as well as a decreased slope in this region. One notable result of these effects is that deviation from predictions is not constant within the linear region. Instead, deviation was least at low currents and near the onset of saturation and greatest approximately midway between these regions. Figure 15 shows a representative example.

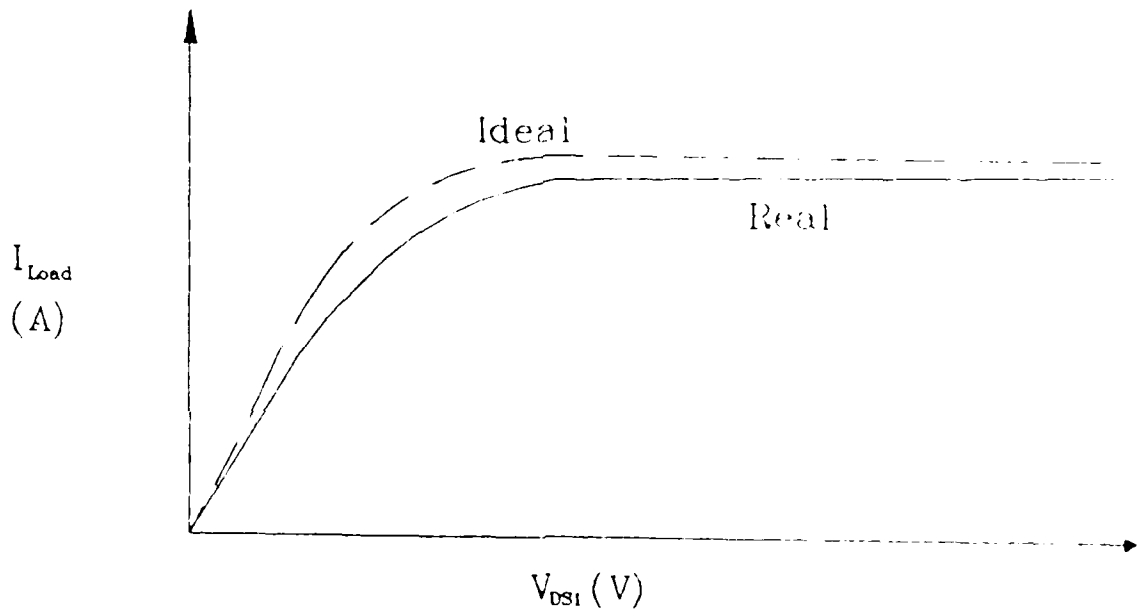


Figure 15: Ideal and Real I-V Characteristics of CMFETs With the Same Gate Bias

These non-idealities can be explained by inadequacies of the simple model The effect of the late onset of saturation is easily explained by noting that a more complex model which accounts for ionic charge variation along the channel predicts such behavior[14]. The lower saturation current is a result of the combination of ionic charge variation and the reduced carrier mobility brought about by the heating of the die from power dissipation which becomes significant at the higher currents typical of saturation in a power MOSFET.

The net effect of these non-idealities was that the radiation response can not be quantitatively explained in a simple fashion using any tractable current-voltage equations. Therefore, although the devices did *qualitatively* obey the form of the simple equations, explanation of the response must be the result of more careful examination than would be the case if the devices were to follow the simple equations more closely.

SECTION 4.1: OPERATION IN THE LINEAR REGION

The results which are of greatest interest are those pertaining to the linear region of operation, because this is the operating mode in which CMFETs are most likely to be used. As a consequence, testing efforts were concentrated on this topic. The resulting data fits the theory quite well, even with the inclusion of some unexpected effects.

The first notable result was the absence of any significant asymmetry in the shifts of threshold voltage under any but the most extreme conditions. A representative plot of threshold voltage shift versus total dose is shown in Figure 16. Using a margin of error of ± 0.05 V for the threshold voltages, the amount of shift was equal for both the load and sense cells, even for the largest sense resistance value (1 kΩ). This means that the sense resistance need not be kept small to avoid such asymmetry, although it may be desirable to do so for other reasons.

The lack of asymmetry is not at all unreasonable when one considers the problem. The magnitude of the electric field in the gate oxide only affects threshold shift in a strong manner over a limited range [12]. At higher magnitudes of electric

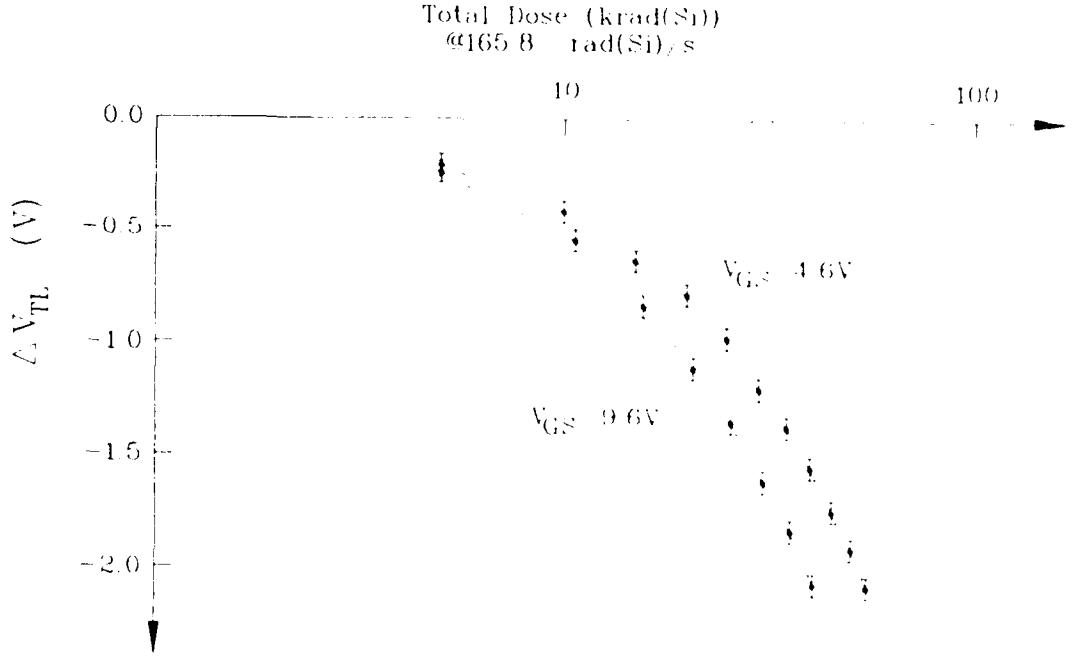


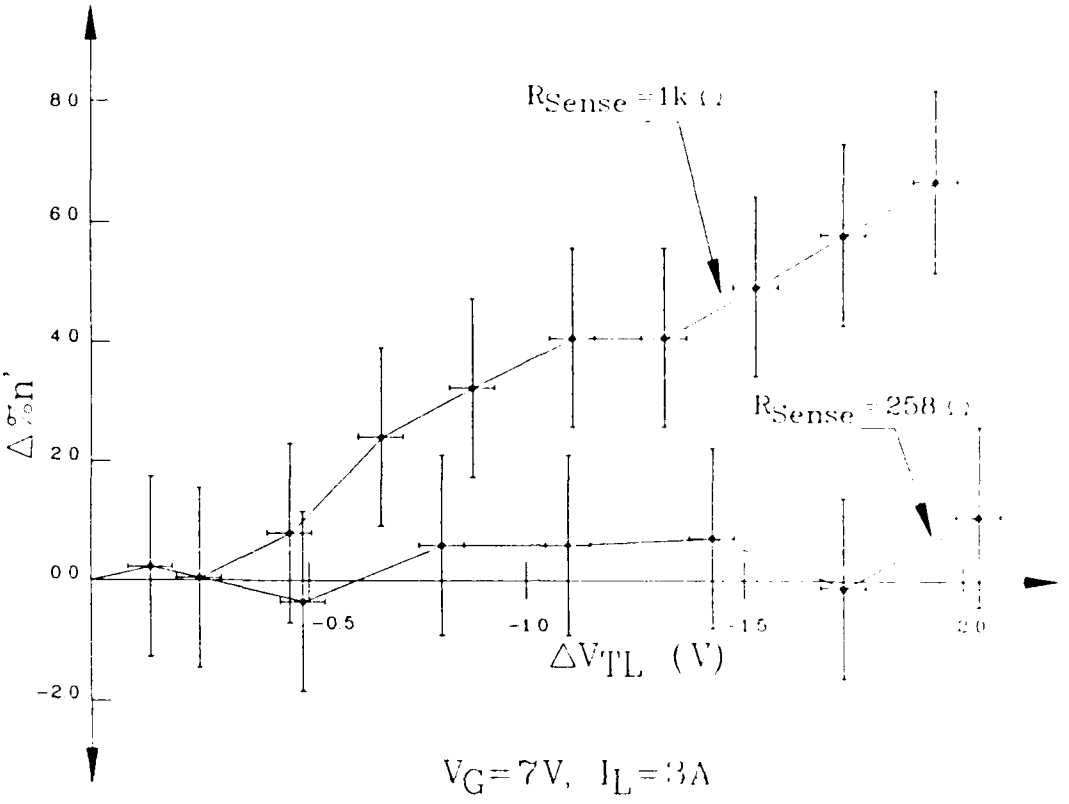
Figure 16: Sample Threshold Shift Data

field, the reduction in initial recombination is not affected much by even higher fields since little recombination is taking place. If this is translated to gate biasing, at a high enough gate bias, a much higher bias is necessary to noticably affect the rate of threshold shift. Add to this the fact that at a high bias level, such as 10 V, even such a high voltage difference as 500 mV means only a difference of 5% between the field in the load gate oxides and the sense gate oxides and it seems quite reasonable that differences in the rate of shifting between these sections would not be noticable.

Another, more unexpected, result was a slight, but noticable asymmetry in the degradation of K_L and K_S. While in a few isolated cases the asymmetry was greater than 10%, for almost all cases the asymmetry was within a few percent. Because no pattern could be established that would allow prediction of the magnitude or direction of this asymmetry, it is believed that this phenomenon is attributable to a combination of measurement error and statistical fluctuations.

The effects on the current ratio, n', were as expected from the first-order analysis under the condition of equally shifting thresholds. When the sense voltage was greater than the parasitic voltage at the load source, n' shifted positively. When the sense voltage was less than the load source potential, n' shifted negatively.

Although the qualitative behavior was as expected, the magnitudes of the observed shifts in n' were very encouraging. The best and worst cases are shown in Figure 17. The worst case situation was when the load section was started near the edge of saturation and with a sense resistance such that a large sense voltage was produced. In such a case, positive shifts in n' of up to 7% were observed for a threshold shift of over 2 V (at 49 krad(Si) total dose). As expected, the best case was for $V_{DS1} \ll V_{GS1} - V_T$ and a small difference between the sense voltage and the parasitic voltage. For the best case, no shifts larger than the margin of error were observed for threshold shifts of almost 2.5 V (at 40 krad(Si) total dose). Equally significant was the result that for small effective sense voltages (the difference between the voltage across the sense resistor and parasitic source lead voltage drop) there were similarly small shifts in n' for any linear region operating conditions. Because the best case conditions are identically those which are most likely to be used, the results show that the current sensing function of CMFET-type



$V_G = 7V$, $I_L = 3A$

For $R_{Sense} = 258\Omega$, $V_{Sense} - V_{Par}$ is approximately 100mV.

For $R_{Sense} = 1k\Omega$, $V_{Sense} - V_{Par}$ is approximately 530mV.

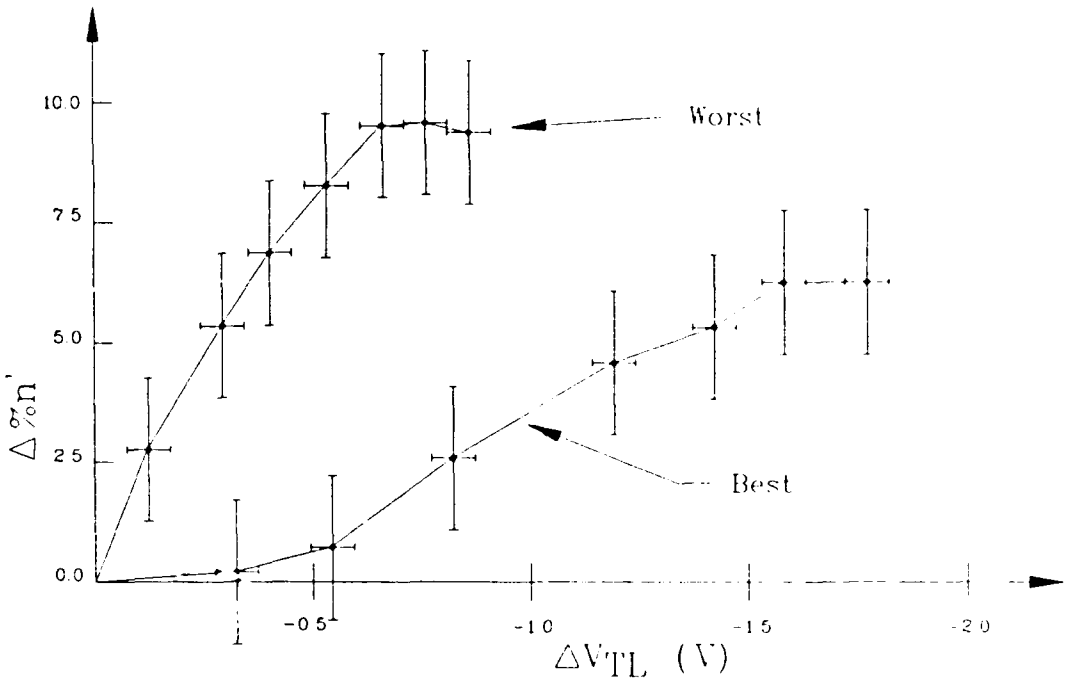
Figure 17: Results for two linearly biased cases

power devices would not be altered in a significant manner by exposure to ionizing radiation at a low dose rate.

SECTION 4.2: OPERATION IN THE DEEP SATURATION REGION

For an initial operating point deep into saturation, the effects on the current ratio n' were very much as expected. There were relatively large positive shifts for the worst case of large effective sense voltage; but, for cases with symmetric threshold shifts, even the worst was less than 7% for nearly two volts of threshold shift (40 krad(Si)) at constant current and less than 10% for constant applied voltages after nearly one volt of threshold shift (26.5 krad(Si)). Figure 18 shows some representative data. For negative effective sense voltages, negative shifts were within a few percent of the initial values. In fact, for the small values of sense resistance and constant applied voltages such that sense voltage is initially lower than the parasitic voltage and the parasitic voltage increases more rapidly with shifts in threshold, the shifting of n' follows an interesting pattern. In such cases, n' initially shifts negatively and then begins to shift positively, surpassing its initial value for a net positive shift. Such a pattern is completely consistent with the theory used in the earlier analysis when thermal effects are also considered, as will be shown.

At the high currents (and drain-source voltages) when the device is in saturation, there is significant heating of the die. This heating causes the channel mobility to lower significantly, lowering the current at the operating point. This lower current also means a higher gate-source voltage because of the lower voltage drops. In terms of the first-order equations, the squared voltage term in the load current equation increases more rapidly than that of the sense current equation, due to the more rapidly decreasing parasitic voltage for given, proportional drops in the two currents. In other words, these equations show that the effect of a rise in temperature is an increase in n'. Thus, there are two competing effects. At lower currents, n' shifts steadily downward as threshold shifts, but as heating becomes significant, the thermal effect on the current ratio counteracts this shift and eventually dominates it resulting in a net upward shift in n'. In the case of a large



Best Case:
Constant Load Current
$R_{Sense} = 289\Omega$

Worst Case:
Constant Applied Voltages
$R_{Sense} = 1k\Omega$

Figure 18: Results for two saturation-biased cases.

sense resistor such that sense voltage is the more rapidly changing voltage, then, the opposite effect should be observed; a negative thermal shift in n' counteracting the normal positive shift. This is precisely what was observed, and the theory was further substantiated for the case of constant current (and die temperature) where no such effect was observed. At constant current, an equivalent of the thermal effect was observed.

The analysis above was also verified using SPICE2G.6 circuit modeling. This was accomplished using the level 1 MOSFET model to simulate the circuit and by changing the appropriate parameters to represent a rise in die temperature. First, the circuit was simulated for room-temperature parameter values and n' was calculated yielding a ratio of the proper order of magnitude. The transconductance parameter KP was then increased by a factor corresponding to die temperature of seventy degrees Celcius (according to the device data sheet information) and the circuit simulation was run again with all other parameters the same as for the intial simulation. The resulting current ratio was found to be higher by about 7%, the proper order of magnitude for correspondence with experimental observation.

With gate-source voltage adjusted to maintain constant current, the degradation of channel mobility from radiation damage had some effect on the current ratio. Although the magnitude of the effects was smaller, it was qualitatively very similar to the effect of rising temperature, because the $V_{GS1} - V_T$ term had to increase slightly to maintain a constant current. Although the situation was different in that the parasitic voltage stayed constant in this case, this served to isolate the effect of channel mobility on the current ratio for operation in the saturated region. Since there was no other competing effect, changes in n' at constant current were monotonic. For small effective sense voltages, n' changed by less than 7% for threshold shifts of 2 V (45 krad(Si)). For large negative effective sense voltages, n' decreased by less than 4%, and for large positive effective sense voltages, n' increased by about 20%. However, the case of large positive effective sense voltages and constant current was the case which exhibited a notable asymmetry in threshold voltage shift and only about 6% of the shift in n' was attributable to effects other than this asymmetry. The similarity in the results from the constant

current experiments serves to confirm the effect of channel mobility degradation since, as predicted, the magnitude of this sense voltage had a negligible effect on the magnitude of the current ratio shift, as far as this effect was concerned.

The results for deep saturation operation can be summarized concisely. When gate voltage was not adjusted to maintain constant load current, current ratio shifts were larger than for those of linear operation with the largest (positive) shifts occurring with large sense resistances and the smallest (positive and negative, depending on the parasitic voltage) with the lower sense resistance values. Although at constant current the changes in n' were comparable to those for linear operation, the magnitude of the shifts was relatively insensitive to the size of the sense resistance. However, although the observed shifts were often larger than for linear operation, they were small enough (especially at constant load current) to still be reasonable for applications which do not require a great deal of precision.

SECTION 4.3: THE OPERATIONAL AMPLIFIER CIRCUIT

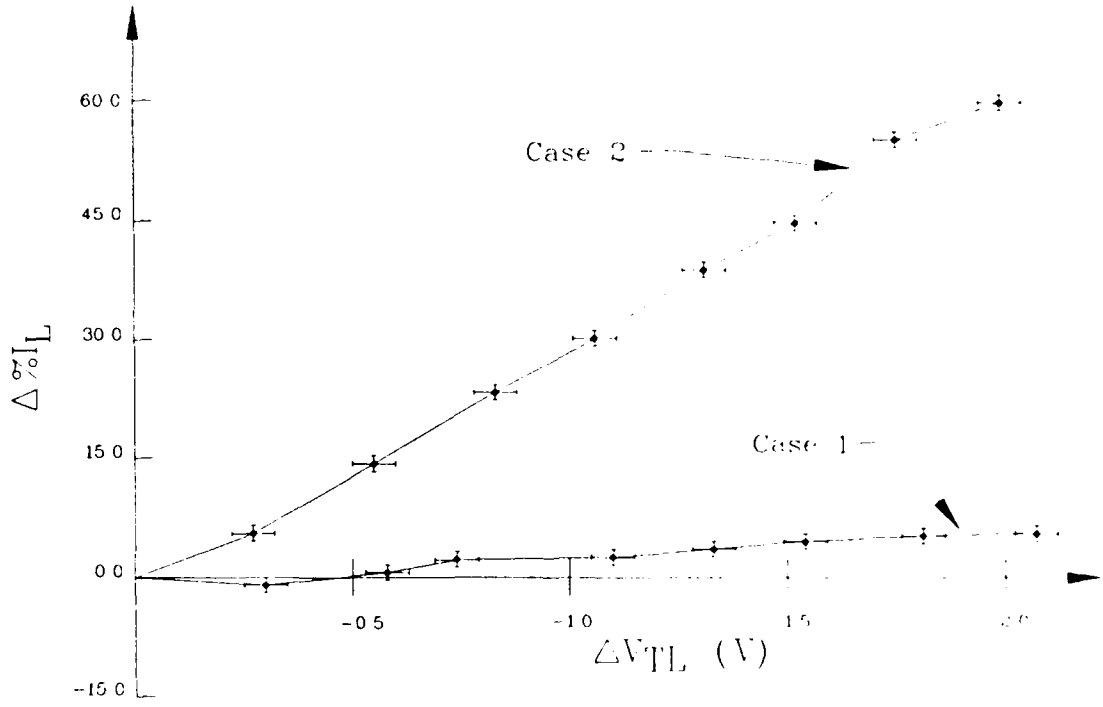
In examining the response of the op-amp circuit to total dose exposure (see Chapter 3), it is worthwhile to note the difference in figures of merit for this experiment, as opposed to those previously described. Although the current ratio is still important, the importance is now secondary in that it is not the end result, but only a means for achieving that result. The real figure of merit for this circuit is the load current, since the circuit is intended to provide a constant load current that would not be possible without the feedback made practical by the near-constant current ratio of the CMFET. Although it is impossible for load current to remain exactly constant in such a circuit, it was shown that it can be held very close to constant under the proper conditions.

The reason a constant current is impossible is the consequence of a basic property of the op-amp itself. The output of the op-amp is simply the input voltage (the difference between V_{ref} and V_{Sense}) multiplied by a constant gain factor. In order to keep a constant current as the threshold voltage drops in response to total radiation dose, the output of the op-amp must drop by the same amount as the

threshold voltage. However, for this to happen, the input voltage must drop by that same amount divided by the closed-loop op-amp gain. The only way this can happen is for V_{Sense} to rise, corresponding to a higher load current.

The amount of shift in load current is a function of the total loop gain. The total loop gain increases as R_{Sense} increases and also as the closed-loop op-amp gain is increased. In other words, higher total loop gain means that it takes a smaller change in sense current (therefore load current as well) to produce the same change in output voltage. The shift in load current is thus reduced as total loop gain increases. Therefore, one chooses high sense resistances and as high as possible a closed-loop gain, short of causing circuit oscillation, in order to minimize the shift from this effect.

A representative choice for this condition ($R_{Sense} = 500\ \Omega$ and $A_{CL} = 100$, where A_{CL} is the closed-loop gain) yielded load current shifts of less than 6.5% for nearly 2 V of threshold shift (40 krad(Si)) attributable mostly to the phenomenon noted above and partially to the small current ratio shift known to occur for this operating condition. On the other hand, for a worst case situation ($R_{Sense} = 50\ \Omega$ and $A_{CL} = 10$), current shift was nearly 60% at the same point. Nonetheless, in almost all cases, the current shift was nearly two orders of magnitude smaller than that which would have taken place for the same threshold shift using constant biasing voltages. (Sample results are shown in Figure 19.) Even though this circuit itself has limited applications, it demonstrates, in principle, both that it is possible to use the current ratio to compensate for total ionizing radiation dose effects and that CMFET-type devices can be used in such an environment without their current-mirroring function being significantly affected.



Case 1: A_{CL}=100, R_{Sense}=500 Ω

Case 2: A_{CL}=10, R_{Sense}=50 Ω

Figure 19: Results from the op amp circuit for two cases of total loop gain

CHAPTER 5: DISCUSSION OF APPLICATIONS

The d.c. biased experiments showed that for many useful operating conditions, current ratio shift was either negligible or still managably small, even after substantial threshold voltage shift (greater than 2.5 V in some cases). Furthermore, the most useful condition (strongly linear) was the one with the lowest shifts, while the next best was strong saturation. It was also shown that the lowest shifts for a given operating condition occur for the lowest values of effective sense resistance (or ordinary sense resistance if parasitic voltage drops are negligible). With these favorable results in mind, it is instructive to briefly consider a few potential applications for CMFET-type devices as a part of PICs and what effect the above results have on determining their suitability for use in radiation environments.

When integrating power and control functions, a wide variety of devices for use on the same die are available. A fabrication process has been developed by AT&T Bell laboratories which provides dielectrically isolated devices which range from a lateral DMOS power transistor to normal MOSFETs and includes other devices such as npn or pnp bipolar transistors and photodiodes [3]. Using such a process, it is possible to create a CMFET and its control circuitry on the same die without worrying about parasitic leakage currents between devices. Switch-mode power supplies, motor controls, and $\dot{\gamma}$ detection and protection (a very important topic in radiation hardening of power MOS devices) are among the integration applications made possible by such a process.

SECTION 5.1: SWITCH-MODE POWER SUPPLIES

One of the most common uses of power MOSFETs is in switch-mode power supplies (SMPS). A basic SMPS is very similar, in principle, to the PWM circuit of Figure 11. The main difference is that the drain current is coupled to a second circuit through a transformer. The second circuit consists of a resistance, capacitance, and inductance network for smoothing the output current or voltage. The PWM circuit is set up so that biasing on the MOSFET gives linear region operation ($V_{GS1} - V_T \gg V_{DS1}$). Since the voltage comparator is used in a digital fashion

(rather than the linear amplification of the op-amp), the circuit is never stable. Instead, the duty cycle of the gate bias is constantly adjusted by the feedback to give a constant average current. The advantage of using a CMFET instead of a normal MOSFET lies in the power efficiency and the non-disruptive nature of its current-sensing function and the opportunity it gives for eliminating an expensive, bulky power resistor.

The experiments performed show that, in such an application, any shift in the current ratio is negligibly small and should not be a concern for the designer, particularly if a small sense resistance can be used. In other words, the circuit designer may take advantage of the unique properties of a CMFET to increase the efficiency of the circuit without degrading the performance in a total-dose radiation environment with respect to the same circuit using a conventional power MOSFET and series power resistor. These results are generally applicable to all CMFETs which are designed as described in Section 1.3, since the total dose response was shown to be a first order circuit effect rather than an effect which is dependent on the details of the processing and layout used to fabricate such a CMFET.

This integration may be taken a step further. Because the major radiation-induced problem for SMPSs occurs when threshold voltage becomes less than the low-state gate voltage, lowering the low-state voltage would extend the total-dose lifetime of the circuit. If the designer can integrate a charge-pumping circuit to lower the low-state gate voltage from its original value to a lower value before it is actually passed to the CMFET gate, on the same die, there could be a pin-for-pin replacement of an ordinary, off-the-shelf CMFET which extends the circuit's lifetime without changing the external circuitry at all [4]. Furthermore, if a radiation hardening process is used for the CMFET to slow the rate of threshold shift, the circuit lifetime may be extended even further (although positive threshold shifts need to be considered since superrecovery tends to be a problem for devices made with such a process [2]). Even if such an implementation should prove to be impractical, it is important to recognize the enhanced capabilities and efficiency available through PICs.

SECTION 5.2: LINEAR MOTOR CONTROL

Another application example is to use the op-amp circuit of Figure 14 as a variable current source for a linear motor drive by using a variable reference voltage. This constant current drives a motor and adjusts itself for changes in motor load and changes in threshold voltage. Again, the use of a CMFET gives greater efficiency and lower cost, and the experiments have shown that such a control application would suffer only small changes in accuracy in a total-dose radiation environment, provided that the op-amp itself does not use MOSFETs. Therefore, in both examples, the CMFET offers cost, power, and space savings without a significant reduction in performance in such an environment.

SECTION 5.3: A DOSE-RATE DETECTION/PROTECTION CIRCUIT

The final, and most significant, application example is that of a CMFET used as an integral $\dot{\gamma}$ detector/protector. The key mechanism for upset by $\dot{\gamma}$ in DMOS devices is second breakdown triggered by the avalanching of photogenerated carriers in a strongly reverse-biased DMOS device [30]. The voltage induced by the avalanche carriers moving through the p body diffusion can turn on the base of the parasitic bipolar transistor that is characteristic of DMOS devices, illustrated in Figure 1. Once the transistor is on, it can go quickly into second breakdown causing damage or destruction of the device if allowed to continue, unmitigated [30]. To protect the device, the drain-source (collector-emitter for the parasitic) bias must be short circuited or the gates must be turned on to dissipate the power throughout the entire device, since the condition is only dangerous when only a few of the most sensitive cells are upset, and all the power is dissipated in them alone. The common method used to guard against such occurences is to derate the amount of reverse voltage is allowed to block to about 30–40% of the rated value. This requires the use of more expensive, less efficient higher-voltage parts.

If the sense cells can be made more sensitive to upset than the load cells, the sense voltage can be used to trigger upset protection. Such a function is desirable

because a detector which has the same characteristics as the device being protected provides the greatest reliability. There are several possible ways to possibly make the sense cells more sensitive to $\dot{\gamma}$ which involve changing the base resistance of the parasitic bipolar transistor. The higher this resistance (assuming no change in minority carrier lifetimes), the greater the susceptibility to $\dot{\gamma}$ upset [30]. Among the simplest ways to achieve a higher base resistance is by simply changing the size of the cells so that base area of the sense cells is greater; this would require a change in the appropriate masks. Although this would change current ratio characteristics, accuracy is not a primary consideration for such an application and, in any case, it is trivial to use a few more cells for more accurate sensing needs, especially if the $\dot{\gamma}$ protection functions are integrated such that no additional external pins are needed.

As an example of such protection, the sense voltage could turn on a bipolar device with the collector connected to the CMFET drain and with a grounded emitter which would short-circuit the drain-source bias when on. A simple resistor-capacitor combination could be used to turn off the bipolar transistor if the RC time constant were longer than the generated carrier lifetime, or the designer could simply use the dropping sense voltage to turn off the base of the bipolar device. Experiments show that when such a circuit is given a large enough $\dot{\gamma}$ to cause damage, the drain-source bias is indeed shorted quickly enough and for long enough to prevent breakdown and subsequent damage. The circuit used in the experiment is shown in Figure 20. Q1 acted as the load device and Q4 as the sense element; both were rated as 500 V parts (IRF420). Q2 and Q3 (MJE16004) were used as the clamping device and the inductor represents the load. An electron linear accelerator (LINAC) was used to simulate $\dot{\gamma}$ (Little Mountain LINAC, Ogden, UT). M1, M2, and M3 were voltage monitors and CT-2 was a current probe. To measure the actual dose-rate, a PIN diode was mounted in front of the test circuit.

Figure 21 shows the relevant results of the testing for a 1 μs pulse at 1.7×10^{10} rad/s. Figure 21a shows that shortly after the pulse, the drain-source voltage was momentarily clamped and then recovered quickly. Figures 21b and 21c show the

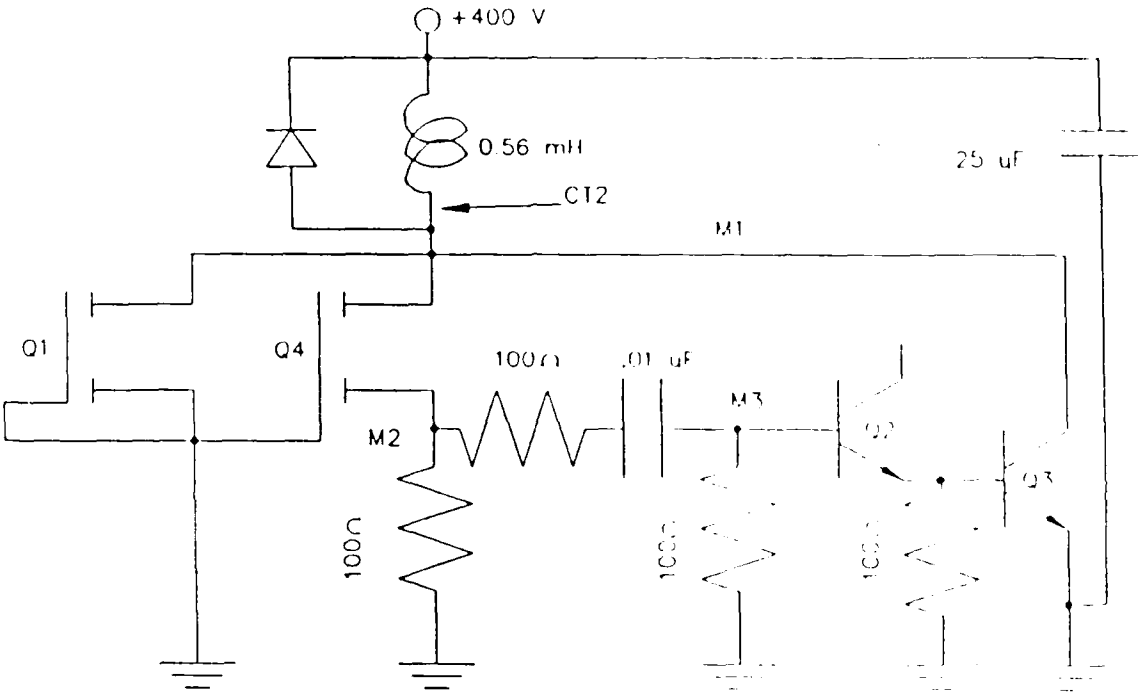


Figure 20: Dose-rate Detection/Protection Circuit

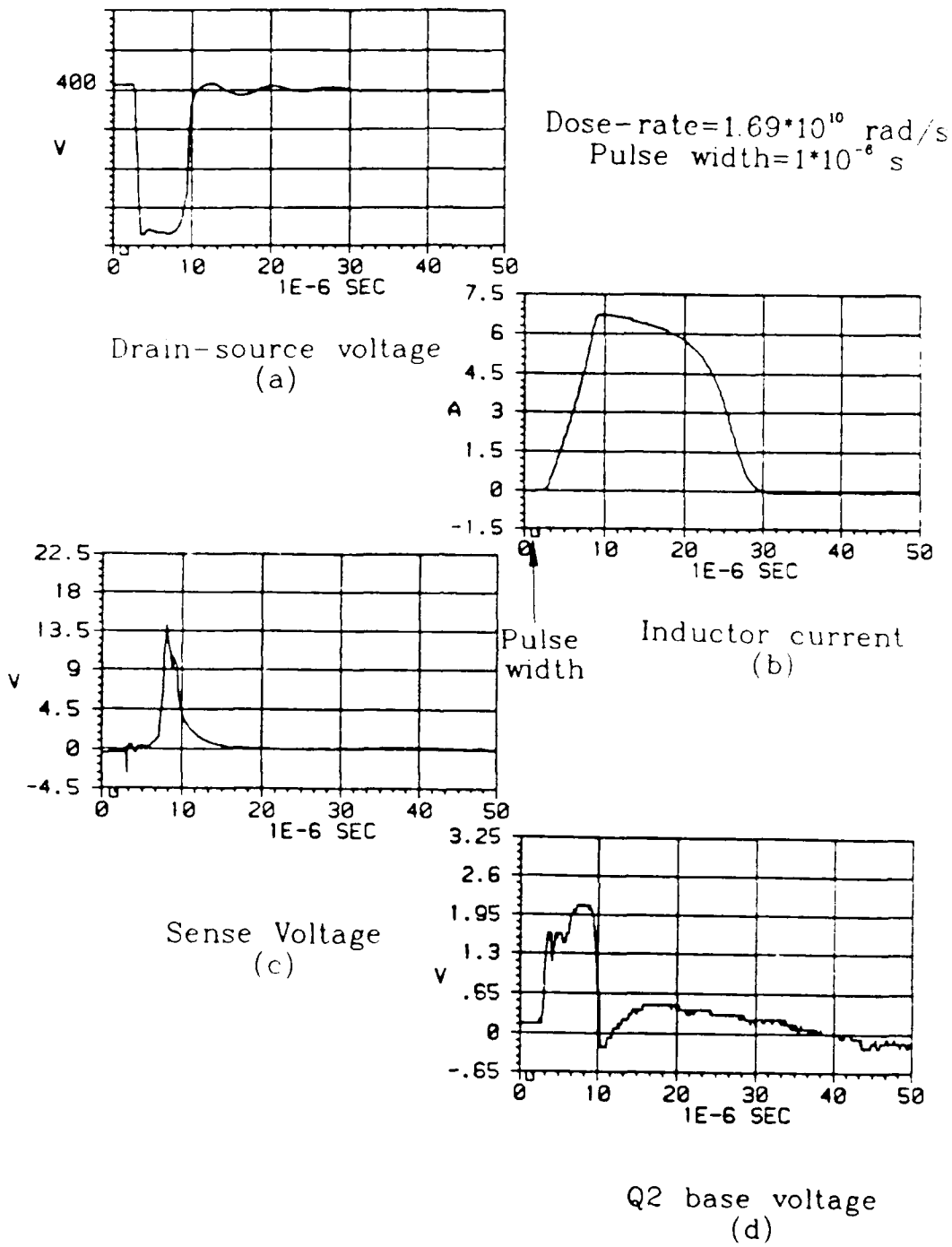
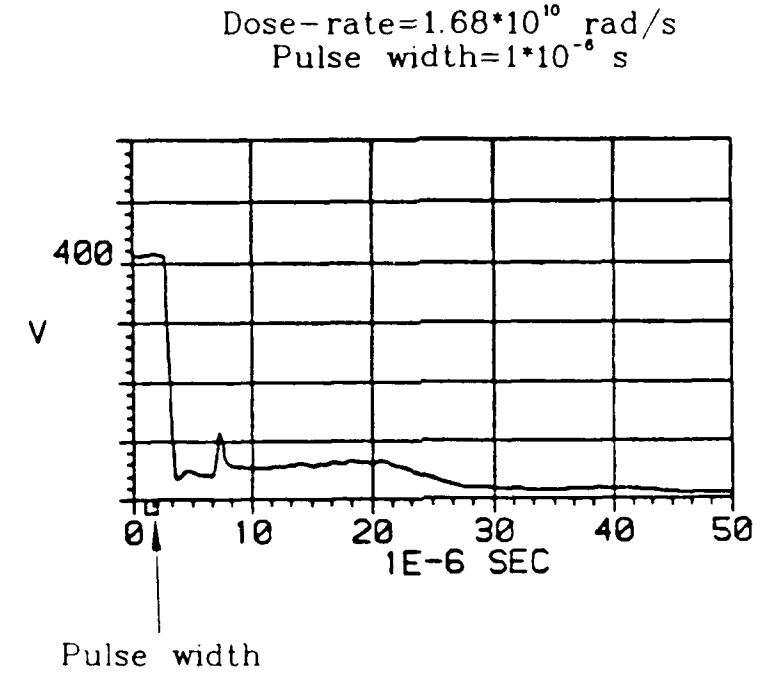


Figure 21 Dose-rate testing results for a MOSFET with protection circuit

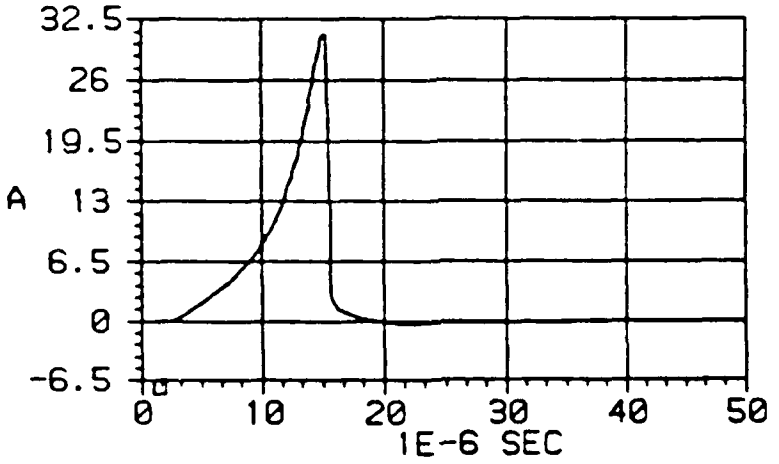
sense voltage and base voltage of Q2, respectively, illustrating how the photocurrent triggers the clamping action. Figure 21d shows the rapid rise in inductor curre which is necessary for the 400 V to be dropped across the inductor during the clamping. None of the parts were damaged during the test.

Figure 22 shows the results for the same pulse given to Q1 without the protection circuit. Figure 22a shows the drain-source voltage collapsing from photocurrent flow without recovery, because transient burnout resulted from the onset of second breakdown. Figure 22b shows the inductor current as it rapidly ran away, signalling second breakdown in the transistor.

The net result, then, is that with the sense element used in a detection/protection circuit, the entire device was protected from transient burnout. Without the protection, the device burned out. This shows that, if such a protection circuit is used, the need for voltage derating for $\dot{\gamma}$ considerations is effectively eliminated. This provides a solution to a radiation hardening problem of major proportions in a cost-effective manner and has the possibility of allowing implementation without external circuitry modifications through fabrication of the entire circuit as a PIC. Such an approach allows enhanced performance, streamlined design, and reduced cost.



Drain-source voltage
(a)



Inductor current
(b)

Figure 22: Dose-rate response of a MOSFET without protective circuitry.

CHAPTER 6: CONCLUSIONS

Radiation tests were conducted on current-mirror MOSFETs, which allow a nearly lossless sensing of load current (defined by a current-ratio n') and are an important element of many PICs. Total-dose radiation testing was performed under d.c. biasing conditions for three different operating conditions and for operation in an op-amp test circuit designed to provide a constant load current.

Strongly linear operation was found to be the best operating condition with respect to the constancy of n', with strong saturation being the second best in most cases. Deep saturation was found to have the greatest potential for problems with n' shifting, depending on circuit conditions. For the best cases, no change in n' was seen, while a change of 20% was the worst observed case. In all cases, shifts in n' were largest when the sense resistance was large and minimal when the sense voltage was approximately equal to the parasitic voltage (equivalent to a very small sense resistance if parasitics are negligible). The op-amp circuit showed minimum current shifts of 6.5% for high total loop gain and a maximum of 60% higher for low total loop gain, both after significant shifts in threshold voltage. The net result of this testing is that, in most cases, designers can take advantage of the benefits of PICs as far as the performance of the current mirror in a total-dose environment is concerned, particularly if sense resistance can be kept small. However, the circuit designer should also be aware that there are cases where current ratio shifts from total-dose exposure may be greater than can be tolerated.

Application examples were also examined using these results and $\dot{\gamma}$ testing results. This examination showed the advantages inherent to using PICs rather than discrete power and control devices. Proposed applications included switch-mode power supplies, linearly variable motor controls, and an integrated dose-rate upset detector/protector. The feasibilty of the motor control circuit was shown using an op-amp feedback-controlled circuit. The feasibility of the dose-rate upset detector/protector was shown experimentally using a discrete device circuit to approximate an integrated circuit version of the circuit. These applications demonstrated that PICs, and CMFET-type devices in particular, can provide at least the same performance as discrete devices in certain radiation environments and, in

some cases, they provide improved performance and longer radiation lifetime. This was shown to be particularly true for the dose-rate upset protection circuit, which showed, conclusively, that a sense voltage can be used to control a voltage-clamping circuit to prevent transient burnout without having to derate the voltage (a significant achievement). For all cases, PICs perform these functions while maintaining a design that is more efficient in volume, cost, and power.

APPENDIX

*** CHANNEL DEFINITION ***

	NAME		SOURCE	
CHAN	V	I	MODE	FCTN
SMU1	VD	ID	V	CONST
SMU2	VG	IG	V	VAR1
SMU3	VIDS	IDS	I	CONST
SMU4				
Vs 1		-----	V	
Vs 2		-----	V	
Vm 1		-----	----	----
Vm 2		-----	----	----

USER FCTN	NAME (UNIT) = EXPRESSION
1	VGG (V) = VG-1.65*VIDS
2	II (ƒA) = ƒ(6*VIDS)

****** SOURCE SET UP ******

	VAR1	VAR2
NAME	VG	
SWEEP MODE	LINEAR	LINEAR
START	2.0000V	
STOP	6.0000V	------
STEP	.0750V	
NO. OF STEP	54	
COMPLIANCE	100.0mA	

CONSTANT		SOURCE	COMPLIANCE
VD	V	2.5000V	100.0mA
IDS	I	.000 A	5.0000V

Load-section threshold voltage program for the HP4145B.

*** CHANNEL DEFINITION ***

	NAME		SOURCE	
CHAN	V	I	MODE	FCTN
SMU1	VD	ID	V	CONST
SMU2	VG	IG	V	VAR1
SMU3	VIDS	IS	COM	CONST
SMU4				
Vs 1		-----	V	
Vs 2		-----	V	
Vm 1		-----	----	----
Vm 2		-----	----	----

USER FCTN	NAME (UNIT) = EXPRESSION
1	SLOPE (ΩR) = ΔID/(ΔVG*/ID)
2	II (/A) = /ID

****** SOURCE SET UP ******

	VAR1	VAR2
NAME	VG	
SWEEP MODE	LINEAR	LINEAR
START	2.0000V	
STOP	6.0000V	------
STEP	.1000V	
NO. OF STEP	41	
COMPLIANCE	10.00mA	

CONSTANT	SOURCE	COMPLIANCE
VD V	10.000V	100.0mA
VIDS COM	.0000V	105.0mA

Sense-section threshold voltage program for the HP4145B.

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